

# SR192 Tutorial:

## SR214 Channel Group Control Parameter Configuration Via A32

### A) Objective

This document intends to clarify the process of configuring SR214 I/O channel group control parameters via A32 register-based access.

### B) SR214 Channel Group Control Register Bit-Maps and Descriptions

**FC7: Voltage Reference Select Register (WRITE only)**

Upper 8 Channels (MSB)								Lower 8 Channels (LSB)							
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
(not used)							0 = select Reference A 1 = select Reference B	(not used)							0 = select Reference A 1 = select Reference B

**\*\* Note:**

The Voltage Reference A/B selection of the FC7 register assigns the threshold settings of either VGRP1, VGRP2 or VGRP3 to the upper and lower 8-channels of the SR214, depending upon the slot location of the SR214 (see table below).

**SR192 Motherboard Voltage Reference Mapping (applies to SR214 only)**

	Module Slots DRA1-DRA6	Module Slots DRB1-DRB3	Module Slots DRB4-DRB6
<b>Voltage Reference A</b>	VGRP1	VGRP1	VGRP1
<b>Voltage Reference B</b>	VGRP2	VGRP2	VGRP3

### FC8: Output/Power Management Register (WRITE only)

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
(not used)				1 = enable memory for MSB	(not used)	1 = enable output drivers for MSB	(not used)					1 = enable memory for LSB	(not used)	1 = enable output drivers for LSB	1 = enable Registered-Mode addressing (EXPECT/MASK/RECORD memories)

**\*\* Note:**

The SCPI command "OUTP:CHAN:STAT ON/OFF" normally sets bits 1 and 9 of the FC8 register on each SR214 globally per TSA or TSB. This SCPI command is typically issued just prior to run-time and, therefore, bits 1 and 9 can be left set to 0 during configuration of the SR214's channel groups.

### FC9: I/O Control Register (WRITE only)

Upper 8 Channels (MSB)							Lower 8 Channels (LSB)								
Input Strobe Signal			Shift Strobe Signal		Output Enable Signal			Input Strobe Signal			Shift Strobe Signal		Output Enable Signal		
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
000 = TSSTrobe1 001 = TSSTrobe2 010 = FCNTL1 011 = FCNTL2 100 = CSTROBE	00 = TSSTrobe1 01 = TSSTrobe2 10 = FCNTL1 11 = FCNTL2	000 = TSENable1 001 = TSENable2 010 = FCNTL1 011 = FCNTL2 100 = CSTROBE 101 = Always Enabled 11X = Never Enabled	000 = TSSTrobe1 001 = TSSTrobe2 010 = FCNTL1 011 = FCNTL2 100 = CSTROBE 101 = Always Enabled 11X = Never Enabled	000 = TSENable1 001 = TSENable2 010 = FCNTL1 011 = FCNTL2 100 = CSTROBE 101 = Always Enabled 11X = Never Enabled	000 = TSSTrobe1 001 = TSSTrobe2 010 = FCNTL1 011 = FCNTL2 100 = CSTROBE	00 = TSSTrobe1 01 = TSSTrobe2 10 = FCNTL1 11 = FCNTL2	000 = TSENable1 001 = TSENable2 010 = FCNTL1 011 = FCNTL2 100 = CSTROBE 101 = Always Enabled 11X = Never Enabled								

**\*\* Note:**

The Input Strobe selection of the SR214's FC9 register must be the same for the upper and lower 8 channels, as this ensures the input data for the upper and lower 8 channels will be captured and compared at the exact same time, thereby producing a single real-time error result.

**FC10: Input Address Delay Control Register (WRITE only)**

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
(not used)															1 = enable Address Delay Register

**\*\* Note:**  
 The SCPI command "INP:ADEL ON/OFF" normally sets the FC10 register on each SR214 globally per TSA or TSB.

**FC12: Algorithm Select and Control Register (WRITE only)**

Upper 8 Channels (MSB)								Lower 8 Channels (LSB)							
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
(not used)		0 = carry-in source is carry-out of next lower 8ch; serial-in source is MSC of current 8ch 1 = carry-in source is always true; serial-in source is LSC of next upper 8ch	1 = enable SERIAL SHIFT register (set to 0 for all other modes)	0001 = MULTIPLEX 0010 = SERIAL 1000 = HOLD (default) 1001 = RTZ (Return to Zero) 1010 = RTO (Return to One) 1011 = RTC (Return to Complement) 1100 = INC1 (Increment by 1) 1101 = INC2 (Increment by 2) 1110 = INC4 (Increment by 4) 1111 = INC8 (Increment by 8)				(not used)		0 = carry-in source is carry-out of next lower 8ch; serial-in source is MSC of current 8ch 1 = carry-in source is always true; serial-in source is LSC of next upper 8ch	1 = enable SERIAL SHIFT register (set to 0 for all other modes)	0001 = MULTIPLEX 0010 = SERIAL 1000 = HOLD (default) 1001 = RTZ (Return to Zero) 1010 = RTO (Return to One) 1011 = RTC (Return to Complement) 1100 = INC1 (Increment by 1) 1101 = INC2 (Increment by 2) 1110 = INC4 (Increment by 4) 1111 = INC8 (Increment by 8)			

**\*\* Note:**  
 Enabling/disabling the SERIAL SHIFT register (bits 4 and 12) for the upper and lower 8 channels must occur in the following order to avoid signal contention: disable-to-enable (0-to-1) must first occur on the least-significant 8 channels; enable-to-disable (1-to-0) must first occur on the most-significant 8 channels.

### FC13: Output Mode, Enable/Strobe Delay Register (WRITE only)

Upper 8 Channels (MSB)								Lower 8 Channels (LSB)							
		Output Mode		Input Strobe Delay		Output Enable Delay				Output Mode		Input Strobe Delay		Output Enable Delay	
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
<i>(not used)</i>		00 = none (SERIAL)		00 = 0 (default)		00 = 0 (default)		<i>(not used)</i>		00 = none (SERIAL)		00 = 0 (default)		00 = 0 (default)	
		01 = CH1 only (SERIAL)		01 = ~5nS		01 = ~5nS				01 = CH1 only (SERIAL)		01 = ~5nS		01 = ~5nS	
		10 = CH1-4 only (MULTIPLEX)		10 = ~10nS		10 = ~10nS				10 = CH1-4 only (MULTIPLEX)		10 = ~10nS		10 = ~10nS	
		11 = CH1-8		11 = ~15nS		11 = ~15nS				11 = CH1-8		11 = ~15nS		11 = ~15nS	

**\*\* Note:**

The "00" and "01" settings for the Output Mode (bits 4&5/12&13) both apply to the SERIAL mode. The least-significant 8-channels of a SERIAL group will always be set to "01", since it is the LSC (Least Significant Channel) of these 8 channels that will output the SERIAL stream. All upper 8-channel portions of the SERIAL group (if any) will be set to "00", since they will serve to supply the carry-in source to the next lower 8-channels and thus not output any data on their LSCs.

### C) Basic A32-Based Programming Procedure - SR214 Channel Group Control Registers

**Step 1:** Use the VISA *viWrite* function to send "ROUT:PATH:DEF <group name>,<channel range>,\*OPC".

(\*\* "ROUT:PATH:DEF" is needed only if using subsequent SCPI-based channel group operations; "\*OPC" should always be used prior to A24/A32).

**Step 2:** Use the VISA *viWrite* function to send the "\*ESR?" query command (this queries the SR192's 8-bit Event Status Register; bit 0 is Operation Complete).

**Step 3:** Use the VISA *viRead* function to attain the returned string from the "\*ESR?" query command. Loop on this function until bit 0 of the ESR goes to a "1".

**Step 4:** Use the VISA *viOut16* function to WRITE 0x7 (Function Code 7) at address 0x40010 (SR192 CPU Function Code Register).

**Step 5:** Use the VISA *viOut16* function to WRITE a 16-bit data value to the SR214's FC7 register at the base address of the appropriate I/O slot (see table below).

**Step 6:** Repeat Step 4 and Step 5 to program each of the remaining 5 registers (FC8, FC9, FC10, FC12 and FC13).

SR192 I/O Slot Base Addresses

SR192 I/O Slot	Base Address (hex)	Base Address (decimal)
DRA1	200000	2097152
DRA2	280000	2621440
DRA3	300000	3145728
DRA4	380000	3670016
DRA5	400000	4194304
DRA6	480000	4718592
DRB1	500000	5242880
DRB2	580000	5767168
DRB3	600000	6291456
DRB4	680000	6815744
DRB5	700000	7340032
DRB6	780000	7864320

### D) A32-Based Register Programming Example - SR214 Channel Group Control Registers

The following A32 programming example will create and configure a 16-channel group, named "GROUP1", on an SR214 module located in slot DRA1. "GROUP1" will be set to the algorithmic SERIAL mode and will attain control characteristics to be described as each register is programmed.

**viWrite** Buffer: "ROUT:PATH:DEF GROUP1,(@1:16);\*OPC"

(assign a name to the channel group – necessary for all subsequent SCPI-based channel group operations; assert the \*OPC command for the subsequent \*ESR? query)

**viWrite** Buffer: "\*ESR?"

(send the \*ESR? Query to check the SR192's Event Status Register)

<b>viRead</b>	Buffer: (variable)		<i>(loop on this function and check for a "1" at bit 0 – the Operation Complete bit of the ESR)</i>
<b>viOut16</b>	Offset: 0x40010	Value: 0x7	<i>(set Function Code 7 into the SR192's CPU Function Code Register)</i>
<b>viOut16</b>	Offset: 0x200000	Value: 0x0	<i>(set Voltage Reference A for upper and lower 8ch)</i>
<b>viOut16</b>	Offset: 0x40010	Value: 0x8	<i>(set Function Code 8 into the SR192's CPU Function Code Register)</i>
<b>viOut16</b>	Offset: 0x200000	Value: 0x808	<i>(enable memories for upper and lower 8 ch)</i>
<b>viOut16</b>	Offset: 0x40010	Value: 0x9	<i>(set Function Code 9 into the SR192's CPU Function Code Register)</i>
<b>viOut16</b>	Offset: 0x200000	Value: 0x2020	<i>(TSENable1 as OUTPUT ENABLE; TSSStrobe1 as SHIFT STROBE; TSSStrobe2 as INPUT STROBE)</i>
<b>viOut16</b>	Offset: 0x40010	Value: 0xA	<i>(set Function Code 10 into the SR192's CPU Function Code Register)</i>
<b>viOut16</b>	Offset: 0x200000	Value: 0x0	<i>(disable Input Address Delay Register)</i>
<b>viOut16</b>	Offset: 0x40010	Value: 0xC	<i>(set Function Code 12 into the SR192's CPU Function Code Register)</i>
<b>viOut16</b>	Offset: 0x200000	Value: 0x1232	<i>(set SERIAL mode; enable SERIAL shift; source for upper 8ch is MSC; source for lower 8ch is LSC of upper 8ch)</i>
<b>viOut16</b>	Offset: 0x40010	Value: 0xD	<i>(set Function Code 13 into the SR192's CPU Function Code Register)</i>
<b>viOut16</b>	Offset: 0x200000	Value: 0x10	<i>(no output for upper 8ch; CH1-only output for lower 8ch; no enable/strobe delays)</i>