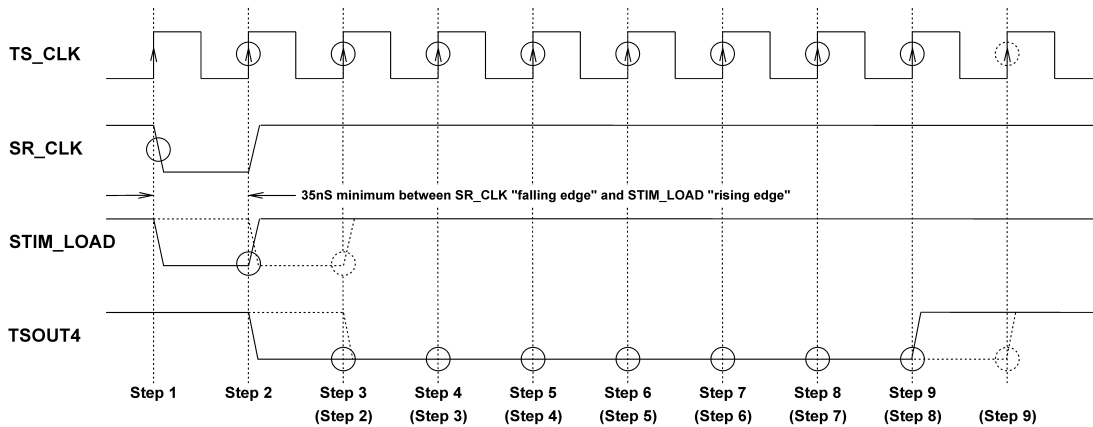
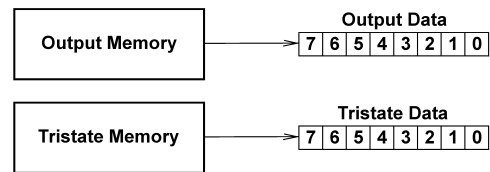


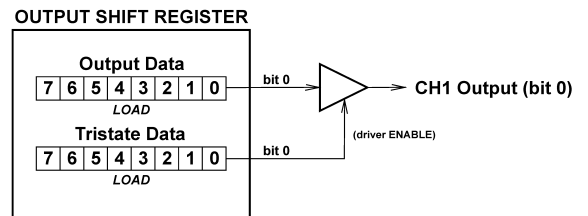
SERIAL Mode: OUTPUT Timing Events (8-bit word shown)



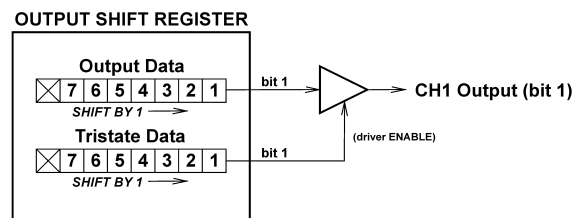
Step 1: SR_CLK "falling edge" increments FMA (Field Memory Address) for Output/Tristate memories. Output/Tristate data is available approximately 30nS from SR_CLK edge.



Step 2: STIM_LOAD "low"/TS_CLK "rising edge" loads Output/Tristate data into output shift register. Bit 0 is output on CH1 driver, which is enabled by Tristate bit 0. "Rising edge" of STIM_LOAD must occur AT LEAST 35nS AFTER "falling edge" of SR_CLK to ensure adequate memory access times (this equates to 2 timing cells between the edges when 28MHz < TS_CLK < 50MHz).

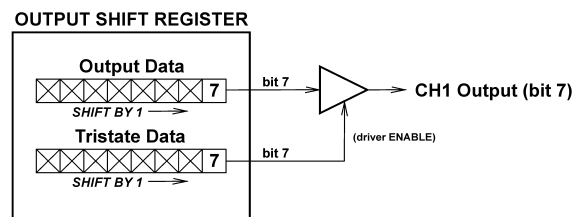


Step 3: TSOUT4 "low"/TS_CLK "rising edge" shifts Output/Tristate data by 1 bit. Bit 1 is output on CH1 driver, which is enabled by Tristate bit 1.

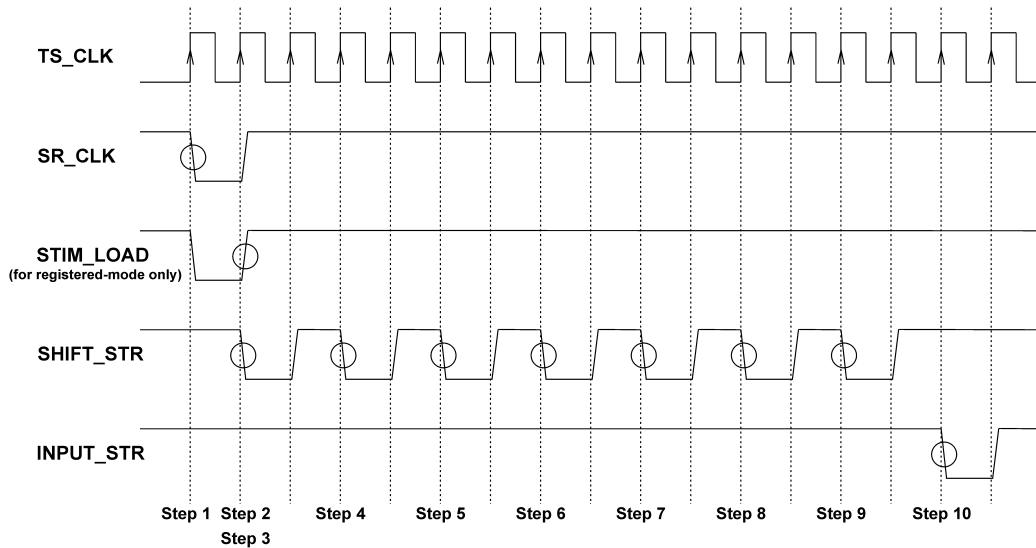


Step 4: ..
Step 5: ..
Step 6: ..
Step 7: ..
Step 8: ..

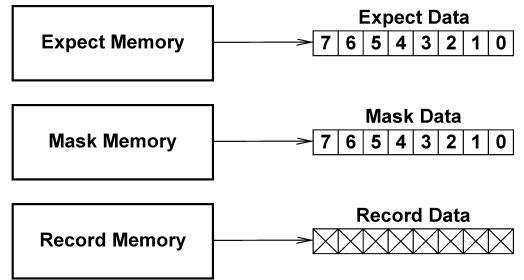
Step 9: TSOUT4 "low"/TS_CLK "rising edge" shifts Output/Tristate data by 1 bit. Bit 7 is output on CH1 driver, which is enabled by Tristate bit 7.



SERIAL Mode: INPUT Timing Events (8-bit word shown)

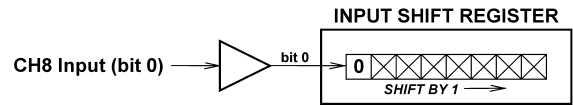


Step 1: SR_CLK "falling edge" increments FMA (Field Memory Address) for Expect/Mask/Record memories. For non-registered-mode groups, Expect and Mask data is available approximately 30nS from SR_CLK "falling edge".



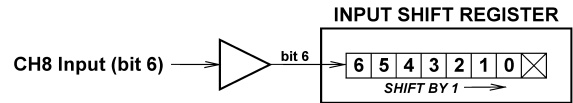
Step 2: For registered-mode groups only, STIM_LOAD "rising edge" registers current FMA for Expect/Mask/Record memories. Expect and Mask data is available approximately 30nS from STIM_LOAD "rising edge".

Step 3: SHIFT_STR "falling edge" shifts bit 0 of CH8 receiver data into input shift register.

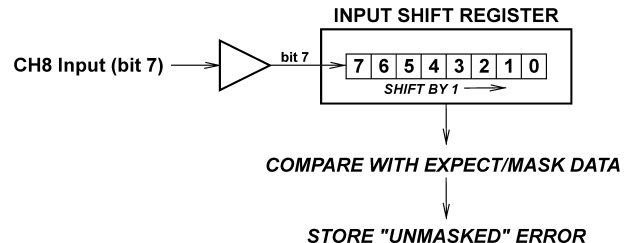


Step 4: ..
Step 5: ..
Step 6: ..
Step 7: ..
Step 8: ..

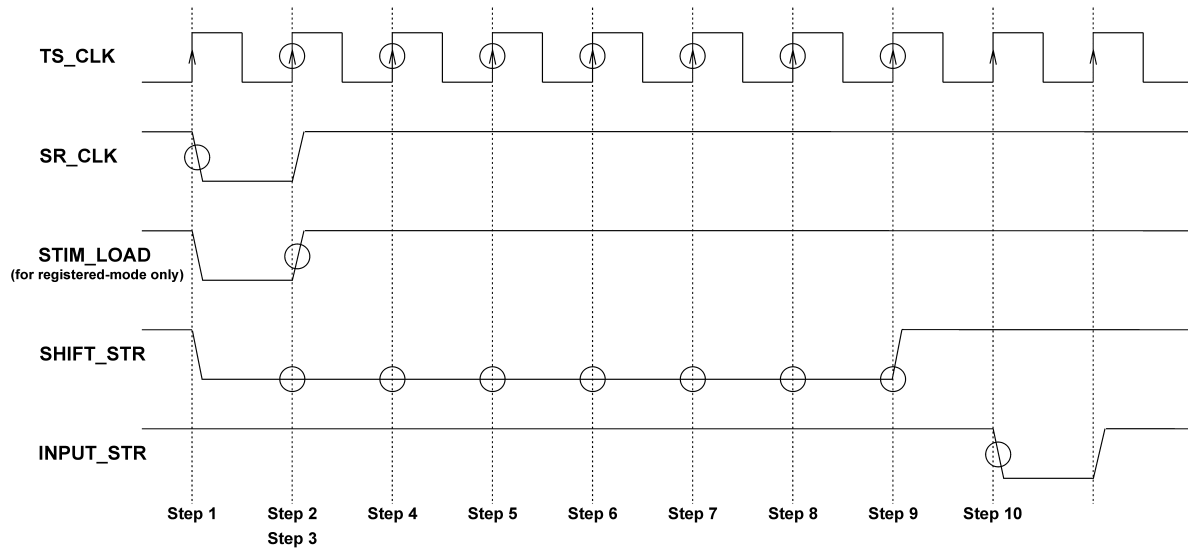
Step 9: SHIFT_STR "falling edge" shifts bit 6 of CH8 receiver data into input shift register.



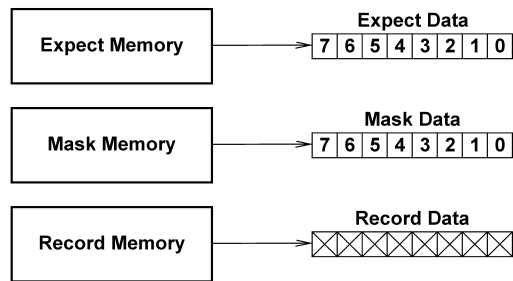
Step 10: INPUT_STR "falling edge": 1) shifts bit 7 of CH8 receiver data into input shift register, 2) initiates real-time compare operation on entire 8-bit word using current Expect/Mask data and 3) stores the "unmasked error" result in Record Memory.



"FAST" SERIAL Mode: INPUT Timing Events (8-bit word shown)

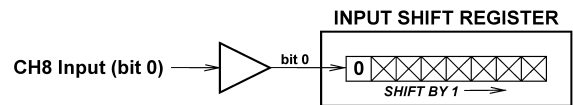


Step 1: SR_CLK "falling edge" increments FMA (Field Memory Address) for Expect/Mask/Record memories. For non-registered-mode groups, Expect and Mask data is available approximately 30nS from SR_CLK "falling edge".



Step 2: For registered-mode groups only, STIM_LOAD "rising edge" registers current FMA for Expect/Mask/Record memories. Expect and Mask data is available approximately 30nS from STIM_LOAD "rising edge".

Step 3: SHIFT_STR "low"/TS_CLK "rising edge" shifts bit 0 of CH8 receiver data into input shift register.



Step 4: ..

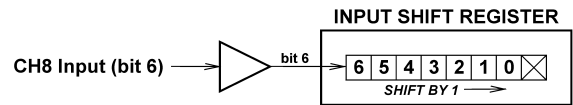
Step 5: ..

Step 6: ..

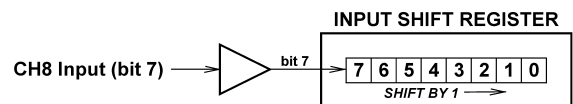
Step 7: ..

Step 8: ..

Step 9: SHIFT_STR "low"/TS_CLK "rising edge" shifts bit 6 of CH8 receiver data into input shift register.



Step 10: INPUT_STR "falling edge": 1) shifts bit 7 of CH8 receiver data into input shift register, 2) initiates real-time compare operation on entire 8-bit word using current Expect/Mask data and 3) stores the "unmasked error" result in Record Memory.



COMPARE WITH EXPECT/MASK DATA

STORE "UNMASKED" ERROR