SR192 Tutorial:

SR101 Control Register 2 (FC9) Command Sequence Via A32

Objective

This document intends to clarify the specific order in which the SR101 Control Register 2 (FC9) commands are issued via A32 register-based access.

Overview

The Sequence/Timing Set Command Register, or Control Register 2, of the SR101 timing module is the register which controls all timing module-based execution cycles aboard the SR192. This is a ***synchronous*** command register, whereby all data written to the register is latched by the selected timing set clock (i.e., TS_CLK). Therefore, if the selected TS_CLK is 10MHz, then Control Register 2 will latch commands every 100nS. For a 1KHz TS_CLK, these commands would be latched every 1mS, and so on.

Control Register 2 for the SR101 is accessed as follows: 1) write 0x9 (i.e., for Function Code 9, or FC9) to the SR192 CPU Function Code Register @ 0x40010 and 2) write the appropriate command(s) to the TSA (@ 0x100000) or TSB (@ 0x180000) Control Register 2.

Control Register 2 Bit Description

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
(not used)		1 = set RUNTS- or CLRWAIT- "high" or "low" as specified by bits 11 and 12.	0 = select RUNTS- 1 = select CLRWAIT- ***** qualified by bit 13 "high" *****	0 = set RUNTS- or CLRWAIT "low" 1 = set RUNTS- or CLRWAIT- "high" ***** qualified by bit 13 "high" *****	1 = set SYNCTS- "low"	1 = set STOP- "low"	1 = set START- "low"	00 = 10MHz 01 = 20MHz 10 = 50MHz 11 = EXTCLK ***** qualified by bit 3 "high" *****		*(not used)*		1 = select new TS_CLK source	*(not used)*	1 = set ENTS- "high"	1 = set ENTS- "low"

ENTS- This "active low" signal sets the timing set address to 0x0, registers the I/O memory contents of FMA location 0 and initiates the IDLE cycle. Since ALL timing set execution must first be preceded by the IDLE cycle, ENTS- must be brought "low" prior to execution. ENTS- set "high" will put the SR101 into its RESET state (i.e., "EXEC:MODE RESET"), thereby stopping the IDLE timing set.

RUNTS- This "active low" signal isolates the CPU address bus from the I/O module FMA bus and the timing module Sequence Address bus, thereby granting FMA "bus master" status to the timing module. During RUNTS- "low", all I/O module memory access is relegated to the timing module and external access is denied.

CLRWAIT- This “active low” signal disables the timing cell WAIT logic and clears any WAIT condition.
START- This “active low” signal initiates the timing module sequencer logic, whereby sequence execution begins with the contents of The First Sequence Register.
STOP- This “active low” signal stops the timing module sequencer logic and forces the timing module into the IDLE cycle.
CLKTS+ This “active high” signal forces the timing module to set the TS_CLK source to the setting specified in bits 6 and 7.
SYNCTS- This “active low” signal initializes the timing cell counter to the first cell of the IDLE timing set, thus synchronizing the IDLE cycles of linked-mode timing modules.

Sequences of FC9 Register Commands for Various Timing Module States

(shown for linked-mode timing operations; otherwise, these are TSA or TSB-specific)

A) To initiate sequence execution after all I/O module and timing module memories have been programmed (IDLE cycle is inactive):

1.	Set CLRWAIT- “low” **(0x3000 to TSA and TSB)**	*This disables the timing cell WAIT logic and clears any WAIT conditions.*
2.	Set CLRWAIT- “high” **(0x3800 to TSA and TSB)**	*This enables the timing cell WAIT logic.*
3.	Set ENTS- “low” **(0x1 to TSA and TSB)**	*This enables the IDLE cycle.*
4.	Set SYNCTS- “low” **(0x400 to TSB only)**	*This synchronizes the IDLE cycles of linked-mode timing modules (if applicable)*
5.	Set RUNTS- “low” **(0x2000 to TSA and TSB)**	*This relegates control of the I/O FMA bus to the timing module.*
6.	Set START- “low” **(0x100 to TSA only)**	*This starts the sequencer, whereby execution begins with the contents of the First Sequence Register.*

B) To stop sequence execution to re-load the I/O memories (IDLE cycle will remain active):

1.	Set STOP- “low” **(0x200 to TSA only)**	*This stops the sequencer, forcing the timing module into the IDLE cycle.*
2.	Set CLRWAIT- “low” **(0x3000 to TSA and TSB)**	*This disables the timing cell WAIT logic and clears any WAIT conditions.*
3.	Set RUNTS- “high” **(0x2800 to TSA and TSB)**	*This relegates control of the I/O FMA bus to the SR192 CPU.*

C) To re-start sequence execution after re-loading the I/O memories (IDLE cycle is active):

1.	Set CLRWAIT- “high” **(0x3800 to TSA and TSB)**	*This enables the timing cell WAIT logic.*
2.	Set RUNTS- “low” **(0x2000 to TSA and TSB)**	*This relegates control of the I/O FMA bus to the timing module.*
3.	Set START- “low” **(0x100 to TSA only)**	*This starts the sequencer, whereby execution begins with the contents of the First Sequence Register.*

D) To stop sequence execution prior to re-loading the timing module memories (IDLE cycle must be inactive):

1.	Set STOP- “low” **(0x200 to TSA only)**	*This stops the sequencer, forcing the timing module into the IDLE cycle.*
2.	Set CLRWAIT- “low” **(0x3000 to TSA and TSB)**	*This disables the timing cell WAIT logic and clears any WAIT conditions.*
3.	Set RUNTS- “high” **(0x2800 to TSA and TSB)**	*This relegates control of the I/O FMA bus to the SR192 CPU.*
4.	Set ENTS- “high” **(0x2 to TSA and TSB)**	*This terminates the IDLE cycle.*