REFERENCE MANUAL

Talon Instruments™

SR210

DAC/Clock/Probe Accessory Module

EADS NORTH AMERICA

Publication Date: 04/25/06
Publication Number: SRMM918 Rev. A
Instrument Part Number: SR210

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- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until performance is checked by qualified personnel.

DOCUMENT CHANGE HISTORY

Revision	Date	Description of Change
A	06/12/2009	Document Control release

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1 Introduction

The SR192 contains two independent stimulus/response digital resources for the VXI bus. Each digital resource contains up to 96 I/O channels and can be run independently or linked to run synchronously. In addition multiple SR192's can be linked through a master/slave configuration.

In addition to the digital resources, the SR192 contains a DAC/MFS slot position that is used for accessory features.

This manual is for the SR210 accessory module. The SR210 provides the following functions:

CLOCK	Two numerically controlled frequency generators can be programmed as UUT clocks. Either of the generators can be selected as the clock source for digital resources.
DAC	The variable voltage I/O modules (SR104, SR114, SR214) require reference signals that determine the output voltages as well as the input compare levels.
PROBE	The SR211 probe pod requires an interface board to send/receive commands as well as record the GOOD0 and GOOD1 data into memory.

The layout of this manual is in five sections described below:

1. Introduction	This section.
2. Specifications	Electrical and environmental specifications of the SR210.
3. Jumpers/Installation	Description of the jumpers and installation of the SR210.
4. Functional Description	Functional description of the SR210 hardware.
5. Memory Data Mapping	Memory to channel mapping

In addition three Appendices are included:

A. Glossary of Terms	Definition of terms used in this manual.
B. Function Code Map	Hardware register description.
C. Programming Examples	SR192 examples using the SR210.

2 Specifications

The following sections list the specifications of the SR210 accessory module.

2.1 Accessory Module

The following sections describe the accessory module specifications.

2.1.1 Clock

Number of programmable clocks ... 2
  PGMCLK1, PGMCLK2
Number of front panel clocks (SMA) ... 3
  CLKA, CLKB, CLKC
Reference Clock
  Internal ... 125MHz
  External ... SMA
  External Input Termination ... 82Ω Parallel to Gnd
CLKA Parameters
  Source ... PGMCLK1
  Delay taps ... 7
  Delay resolution ... 5ns +/- 1ns
  Driver ... 74FCT240
  Termination ... 47Ω Series
CLKB Parameters
  Source ... PGMCLK2
  Delay taps ... 7
  Delay resolution ... 5ns +/- 1ns
  Driver ... 74FCT240
  Termination ... 47Ω Series
CLKC Parameters
  Source ... PGMCLK2
  Maximum high voltage ... +8V
  Maximum low voltage ... -8V
  Driver ... EL1056
  Termination ... 47Ω Series
Minimum Frequency ... 100Hz
Maximum Frequency
  CLKA/CLKB ... 50MHz
  CLKC (VOH - VOL) < 3V ... 50MHZ
  CLKC 3V < (VOH - VOL) < 6V ... 30MHz
  CLKC 6V < (VOH - VOL) < 10V ... 10MHz
  CLKC 10V < (VOH - VOL) < 16V ... 5MHz
Resolution ... 0.0291Hz
Accuracy Error ... <1%
Duty Cycle ... 50%
Jitter
  Clock < 5MHz ... <1%
  Clock > 5MHz ... < 2ns

2.1.2 DAC Reference

Number of reference groups ... 4
  VGRP1, VGRP2, VGRP3, VGRPCLK
Number of channels per group[1] ... 5
  VOH, VOL, VIH, VIL, VISR
Maximum Voltage[2]
  VOH, VOL, VIH, VIL ... +15V
  VISR ... +8V
Minimum Voltage[2]
  VOH, VOL, VIH, VIL ... -15V
  VISR ... -8V
Resolution ... 10mV
Accuracy Error ... < 50mV
Voltage Drift ... +/- 5mV

Settling Time .... < 3 Seconds

Note 1: The VGRPCLK group only has three references, VOH, VOL, VISR.

Note 2: Valid minimum and maximum voltage settings differ and are determined by the I/O module type.

2.1.3 Probe

Timing Module Link .... TSA

Input Memory (GOOD0, GOOD1) 131072

Input Strobe

- Source 5
- TSOUTA5, TSSTROBEA1, TSSTROBEA2, FCNTL1, FCNTL2
- Delay taps 7
- Delay Resolution .... 5ns +/- 1ns

2.2 Electrical

CLKA, CLKB

- High Level Output Voltage .... 2.4V min
- High Level Source Current.. 30 mA
- Low Level Output Voltage .... 0.4V max
- Low Level Sink Current.. 50 mA
- Output Impedance (with 47Ω series terminator) .... 50Ω typ
- Short Circuit Protected.. Yes[1]

CLKC

- High Level Output Voltage .... -8.0V to +8.0V
- High Level Source Current.. 50 mA
- Low Level Output Voltage .... -8.0V to +8.0V
- Low Level Sink Current.. 50 mA
- Voltage Swing 16V
- Output impedance (with 47Ω series terminator) .... 50Ω typ
- Output Slew Rate .... 1V/ns typ
- Short Circuit Protected .... Yes

CLKREF

- High Input Threshold.. 2.0V
- Low Input Threshold 0.8V
- Input Impedance .... > 10KΩ

Note 1: With the 47Ω series terminator installed.

2.3 Timing Characteristics

In order to specify the timing characteristics of the SR210, the TS_CLK signal generated by the timing module will be used as the reference signal. Appendix D of this manual gives the timing relationship between the external input clocks (EXCLK1 and EXCLK2), TS_CLK and external output clocks (CLOCKA and CLOCKB).

Table 2-1 lists the typical timing characteristics of the SR210's probe response logic.

Parameter and Description	From	To	Typ (ns)	Note
Probe Specifications				
Probe propagation delay	Probe Tip	Probe Data Valid	45	-
Internal probe strobe delay	TS_CLK	Internal Probe Strobe	16	1,2
Field control one to probe strobe	FCNTL1-TTL	Probe Strobe	23	2
	FCNTL1-PROG		29	2
	FCNTL1-DIFF		57	2
Field control two to probe strobe	FCNTL2	Probe Strobe	25	2
Data valid setup to response strobes	Probe Data Valid	Probe Strobe	5	-

Note 1: The internal strobes are generated by the TSA timing module (TSOUT5, TSSTROBE1 and TSSTROBE2).

Note 2: Values are listed with the strobe delay set to zero.

Table 2-1 SR210 Timing Characteristics

2.4 Environmental

Temperature Range

Operating .... 0° C to +50° C
Storage .... -40° C to +71° C (RH not controlled)

Altitude

Operating .... Sea level to 10,000 ft.
Storage .... Sea level to 40,000 ft.

Relative Humidity (non condensing)

0°C to +10°C .... not controlled
+11°C to +30°C .... 95+/-5%RH
+31°C to +40°C .... 75+/-5%RH
+41°C to +50°C .... 45+/-5%RH

2.5 Size

Dimension

4.93 cm x 22.61 cm (1.94" x 8.9")

Weight

.074 kg (2.6 oz)

2.6 Power Requirements

The power requirements listed in table 2-2 are for the SR210.

Voltage	Peak Current	Dynamic Current	Note
+5V	475mA	20mA	-
-5.2V	0	0	-
-2V	0	0	-
+12V	100mA	20mA	-
-12V	90mA	14mA	-
+24V	15mA (210mA)	5mA (20mA)	1
-24V	11mA (120mA)	5mA (20mA)	1
V+	0	0	-
V-	0	0	-

Note 1: The values inside the parenthesis include the SR211 probe pod.

Table 2-2 SR210 Voltage Requirements

3 Jumpers/Installation

The SR210 accessory module requires SR192 system firmware revision 1.31 or later for proper operation. Contact Talon Instruments for information on firmware upgrades.

The SR211 probe interface and front panel programmable clocks are only available with SR192 motherboard PCB part number 20231.

Figure 3-1 below is a locator diagram for test points and jumpers located on the SR210.

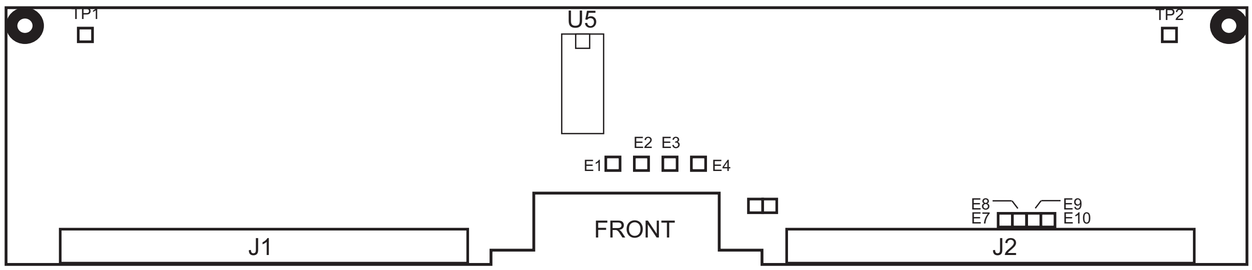


Figure 3-1 Test Point/Jumper Locations

3.1 Test Point Description

Table 3-1 describes the test points on the SR210 accessory module.

Test Point	Mnemonic	Description
TP1	GND1	Signal Ground

Table 3-1 SR210 Test Point Description

3.2 Jumper Description

The following sections describe the SR210 jumper options.

3.2.1 SR210-001 Option Jumper Configuration

The SR210-001 option routes the programmable clock and probe power signals to the front panel via the SR192 motherboard.

E1, E10 — This set of jumpers connect the CLKB and its GND return to the front panel via the motherboard. E1 to J101-5 and E10 to J2-29 installed connects CLKB to the SR192 Front Panel.

E2, E8 — This set of jumpers connect the CLKA and its GND return to the front panel via the motherboard. E2 to J101-7 and E8 to J2-33 installed connects CLKA to the SR192 Front Panel.

E3, E9 — This set of jumpers connect the CLKC and its GND return to the front panel via the motherboard. E3 to J101-9 and E9 to J2-31 installed connects CLKC to the SR192 Front Panel.

E4, E7 — This set of jumpers connect the CLKREF and its GND return to the front panel via the motherboard. E4 to J101-11 and E7 to J2-35 installed connects CLKREF to the SR192 Front Panel.

E5, E6 — This set of jumpers connect the fused -24V signal to the front panel via the motherboard. E5 to E6 installed connects -24VSAFE to the SR192 Front Panel.

CAUTION
The SR210 PCB is manufactured with traces connecting the jumpers described above.

WARNING
The SR210-001 option can only be installed in SR192 motherboards labeled with a PCB assembly number 20231.

3.2.2 SR210-002 Option Jumper Configuration

The SR210-002 option disconnects the programmable clock and probe power signals from the front panel.

E1, E10 — This set of jumpers disconnect the CLKB and its GND return from the front panel via the motherboard. E1 to J101-5 and E10 to J2-29 open disconnects CLKB from the SR192 Front Panel.

E2, E8 — This set of jumpers disconnect the CLKA and its GND return from the front panel. E2 to J101-7 and E8 to J2-33 open disconnects CLKA from the SR192 Front Panel.

E3, E9 — This set of jumpers disconnect the CLKC and its GND return from the front panel. E3 to J101-9 and E9 to J2-31 open disconnects CLKC from the SR192 Front Panel.

E4, E7 — This set of jumpers disconnect the CLKREF and its GND return from the front panel. E4 to J101-11 and E7 to J2-35 open disconnects CLKREF from the SR192 Front Panel.

E5, E6 — This set of jumpers disconnect the fused +24V signal from the front panel. E5 to E6 open disconnects +24VSAFE from the SR192 Front Panel.

CAUTION
The SR210 PCB is manufactured with traces connecting the jumpers described above and must be cut.

3.3 Installation

Each SR192 motherboard can house up to twelve I/O modules, two timing modules and one accessory module. I/O modules are installed in motherboard slots DRA1 through DRA6 and DRB1 through DRB6. Timing modules are installed in slots TSA and TSB. Accessory modules are installed in the MFC/DAC slot, see Figure 3-2.

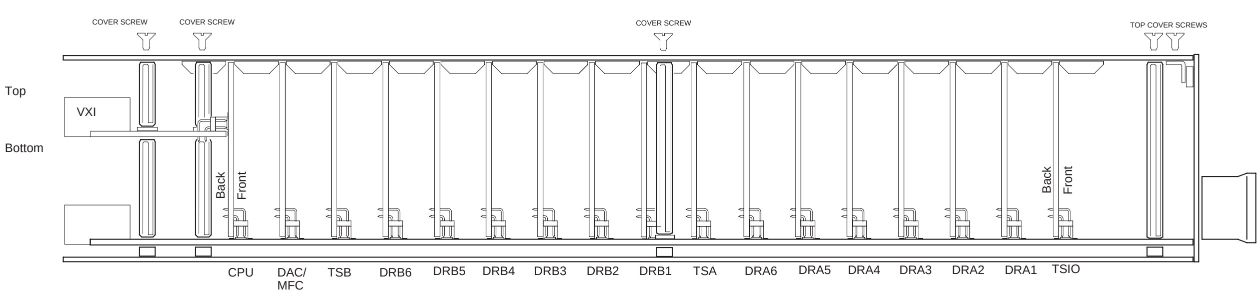


Figure 3-2 SR192 Motherboard Side View

Perform the following steps to add or replace an I/O module:

Step 1. Using ESD protocols remove the SR192 from the VXI chassis.

Step 2. Remove the top cover screws, refer to Figure 3-2.

Step 3. If replacing a module, remove it by grasping at each corner and gently rocking forward and back while pulling it away from the motherboard.

Step 4. Insert the module in the appropriate slot, Figure 3-2, by lining up the J1 and J2 connectors with the motherboard connectors and gently pushing down. All SR192 modules are keyed along the associated mating connector. If the module cannot be inserted, make sure you are inserting the module into the correct slot, check for bent pins and make certain the pins are aligned with the mating connector on the motherboard.

CAUTION

Although the modules and the associated mating connectors have been keyed, it is possible to force a module into an incorrect slot.

Step 5. Reinstall spacers and washers if applicable.

Step 6. Reinstall top cover.

3.4 Termination Options

The SR210 is shipped from the factory with 47Ω series termination resistors on each clock channel. These resisters are installed in U5, see figure 3-1.

U5 is a sixteen pin dip resister package, Bourns part number 4116R-001-470. The resistor pack can be changed by the user.

4 Functional Description

The SR210 accessory module is a multi-function accessory module for the SR192 that includes programmable clock, DAC and probe logic.

The programmable clock logic generates two independent clock that are routed to the front panel as well as the digital resource timing modules.

The DAC logic generates the high and low reference levels for the variable voltage I/O modules.

The probe logic is linked to the timing module for digital resource A and allows the SR210 to record probe data from the SR211 probe pod.

Figure 4-1 depicts the SR210 module in relation to other components of the SR192.

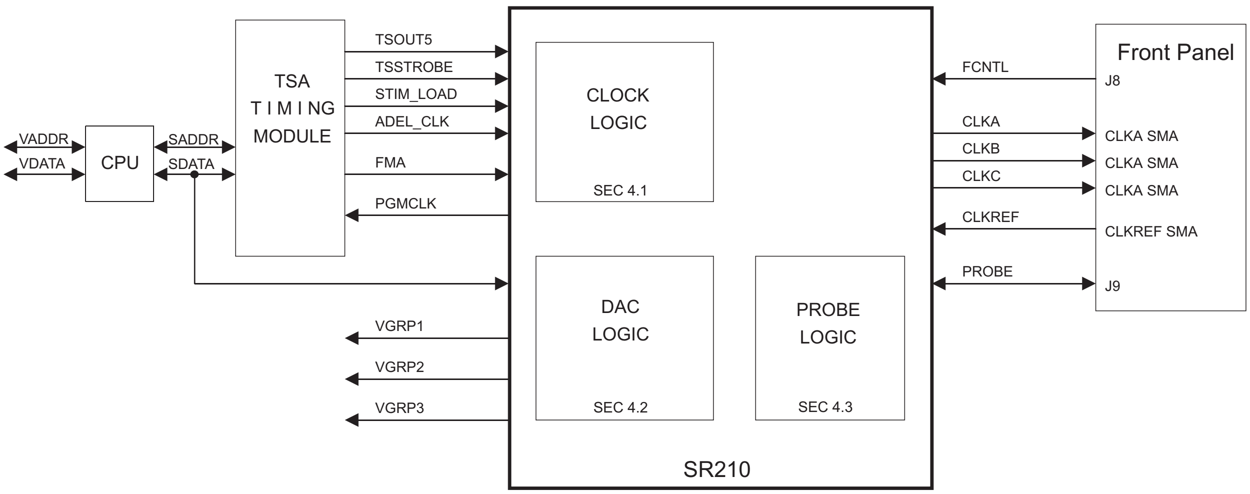


Figure 4-1 SR210 Block Diagram

The following list describes the functional blocks shown in figure 4-1 above.

1. CPU — The SR192 CPU module selects whether the local processor or VXI Backplane has control of the system bus, SADDR and SDATA.
2. TSA TIMING MODULE — SR192 TSA timing module, SR100 or SR101.
3. CLOCK LOGIC — The registers and control bits that generate the programmable clocks (PGMCLK1 and PGMCLK2).
4. DAC LOGIC — The registers and control bits that generate the voltage group references (VOH, VOL, VIL, VIH and VISR).
5. PROBE LOGIC — The interface logic and memory to support the SR211 probe pod.
6. FRONT PANEL — The mating connectors through which a physical connection is made to the UUT.

The following list describes the signals shown in figure 4-1 above.

1. VADDR — The address bus from the VXI Backplane.
2. VDATA — The data bus from the VXI Backplane.
3. SADDR — Either the local microprocessor or VADDR bus.
4. SDATA — Either the local microprocessor or VDATA bus.
5. TSOUT5 — TSA timing module signal which can be selected to strobe probe data.
6. TSSTROBE — TSA timing module signals which can be selected to strobe probe data.
7. STIM_LOAD — TSA timing module signal used to delay the memory address to the probe memory for the output register.
8. ADEL_CLK — TSA timing module signal used to delay the memory address to the record memory for the address delay mode.
9. FMA — TSA Field Memory Address. The FMA selects the stimulus/response memory word.
10. PGMCLK — The selected programmable timing module clock.
11. VGRP1 — Voltage group one references (VOH1, VOL1, VIH1, VIL1 and VISR1).
12. VGRP2 — Voltage group two references (VOH2, VOL2, VIH2, VIL2 and VISR2).

13. VGRP3 — Voltage group three references (VOH3, VOL3, VIH3, VIL3 and VISR3).
14. FCNTL — Two front panel input signals that can be selected to strobe probe data.
15. CLKA — Front panel output signal PGMCLK1, TTL levels.
16. CLKB — Front panel output signal PGMCLK2, TTL levels.
17. CLKC — Front panel output signal PGMCLK2, +8, -8 programmable levels.
18. CLKREF — Front panel input signal, external reference signal for the clock generator.
19. PROBE — Front panel signals that connect the SR211 Probe Pod to the SR192.

The following sections describe the three logic elements of the SR210 (Clock, DAC and Probe).

4.1 Clock Logic

Figure 4-2 shows the clock logic block diagram.

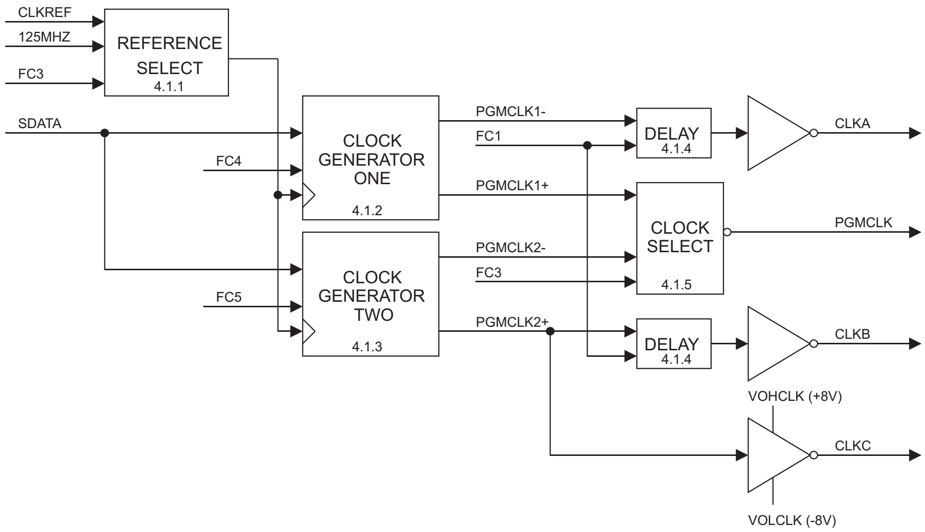


Figure 4-2 Clock Logic Block Diagram

The following list describes the functional blocks of figure 4-2.

1. REFERENCE SELECT — Used to select the reference clock source for the clock generators.
2. CLOCK GENERATOR ONE — One of two clock generators.
3. CLOCK GENERATOR TWO — One of two clock generators.
4. DELAY — Delay logic for the clock output.
5. CLOCK SELECT — Used to select the clock source for the timing modules.

The following list describes the signals shown in figure 4-2 above.

1. CLKREF — Front panel input signal (from the CLKREF SMA connector) that can be selected as the clock generator reference.
2. 125MHZ — Internal signal that can be selected as the clock generator reference (PON default).
3. FC3 — Control signals used to program the reference and clock select signal. Refer to appendix B.
4. SDATA — The selected data bus used to program and query the SR210 registers and memory.
5. FC4 — Control signal used to program the PGMCLK1 frequency. Refer to appendix B.
6. FC5 — Control signal used to program the PGMCLK2 frequency. Refer to appendix B.
7. PGMCLK1- — Inverted programmable clock one signal routed to CLKA.
8. FC1 — Control signal used to program the CLKA and CLKB delay. Refer to appendix B.
9. PGMCLK1+ — Non-inverted programmable clock one signal routed to the timing module clock selector.
10. PGMCLK2- — Inverted programmable clock two signal routed to the timing module clock selector.
11. PGMCLK2+ — Non-inverted programmable clock two signal routed to CLKB and CLKC.
12. VOHCLK — Output high level for CLKC.
13. VOLCLK — Output low level for CLKC.
14. CLKA — Front panel SMA TTL clock (PGMCLK1).
15. PGMCLK — Timing module clock source for both digital resources.
16. CLKB — Front panel SMA TTL clock (PGMCLK2).
17. CLKC — Front panel SMA variable voltage clock (PGMCLK2).

4.1.1 Reference Select

The reference select logic allows the user to select the programmable clock reference signal.

The reference signal must be 125MHz.

4.1.2 Clock Generator One

The clock generator one logic allows the user to program the frequency of the PGMCLK1 signal. The PGMCLK1 signal is routed to CLKA on the front panel as well as the timing module clock select logic, refer to section 4.1.5.

Clock generator one can be programmed from 100Hz to 50MHz.

4.1.3 Clock Generator Two

The clock generator two logic allows the user to program the frequency of the PGMCLK2 signal. The PGMCLK2 signal is routed to CLKB and CLKC on the front panel as well as the timing module clock select logic, refer to section 4.1.5.

Clock generator two can be programmed from 100Hz to 50MHz.

CAUTION

CLKC frequency is restricted based on the voltage swing between VOH and VOL.

4.1.4 Delay Logic

The delay logic allows the user to delay the CLKA/CLKB signal up to 28ns in 5ns increments.

4.1.5 Clock Select Logic

The clock select logic allows the user to select which clock generator to be routed to the timing modules.

4.2 DAC Logic

Figure 4-3 shows the DAC logic block diagram.

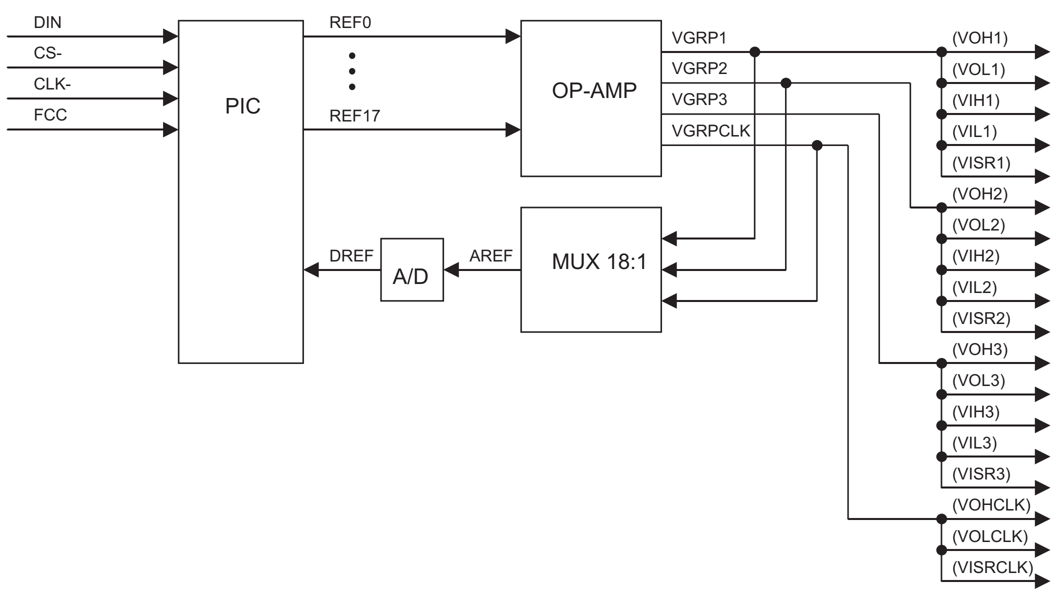


Figure 4-3 DAC Logic Block Diagram

The following list describes the functional blocks of figure 4-3.

1. PIC — Used to program and monitor the references.
2. OP-AMP — Logic used to amplify the reference signal from the PIC.

3. MUX 18:1 — 18 to 1 multiplexer controlled by the PIC to select a reference to monitor.
4. AD — Analog to digital converter converts the selected analog reference to a digital reference for the PIC.

The following list describes the signals shown in figure 4-3 above.

1. DIN — PIC data in signal used for programming.
2. CS — PIC chip select used for programming.
3. CLK — PIC clock signal used for programming.
4. FCC — Function code used to program the DAC logic.
5. REF0 - REF17 — Eighteen reference signals combined into four voltage groups.Front panel input signal (one for each I/O module) that can be selected to either enable stimulus or strobe response data.
6. VGRP1 — Voltage group one references.
7. VGRP2 — Voltage group two references.
8. VGRP3 — Voltage group three references.
9. VGRPCLK — Voltage group four routed to CLKC programmable driver.
10. AREF — Selected analog reference to evaluate.
11. DREF — converted analog reference for the PIC.

The DAC logic is used to monitor and control the 18 reference signals. The DAC operates by selecting each reference one at a time through the MUX and compares the current voltage with the programmed voltage. The PIC will then compensate the reference if the two voltages differ by more than 10mV.

4.3 Probe Logic

Figure 4-4 shows the probe logic block diagram.

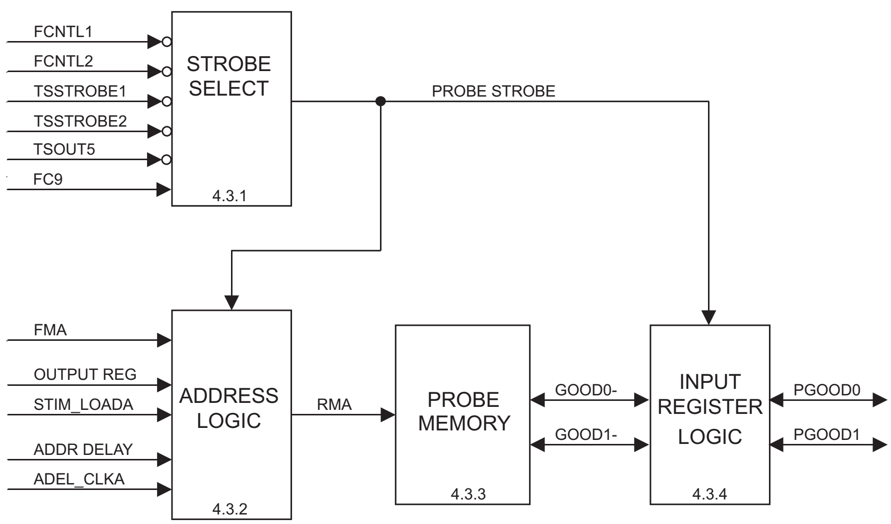


Figure 4-4 Probe Logic Block Diagram

The following list describes the functional blocks of figure 4-4.

1. STROBE SELECT — Used to select and delay the probe strobe signal.
2. ADDRESS LOGIC — A series of registers used to delay the FMA in order to generate a synchronous address to the probe memory.
3. PROBE MEMORY — 128K by 8 memory used to store the GOOD0 and GOOD1 data from the SR211 probe.
4. INPUT REGISTER LOGIC — Logic to register the probe data and generate a write pulse to the memory.

The following list describes the signals shown in figure 4-4 above.

1. FCNTL1 — Front panel input signal (from the J8 connector) that can be selected to strobe probe data.
2. FCNTL2 — Front panel input signal (from the J8 connector) that can be selected to strobe probe data.
3. TSSTROBE1 — Timing Set Strobe 1 from the timing module that can be selected to strobe probe data.
4. TSSTROBE2 — Timing Set Strobe 2 from the timing module that can be selected to strobe probe data.
5. TSOUT5 — Timing Set Output 5 that can be selected to strobe probe data.

6. FC9 — Control signals used to program the probe strobe selector as well as the delay value. Refer to appendix B.
7. FMA — TSA Field Memory Address. The FMA selects the stimulus/response memory word.
8. OUTPUT REG — TSA signal used to indicate if the output register mode is enabled or disabled.
9. STIM_LOADA — TSA timing module signal from TSA that latches the stimulus address bus (FMA) when the output register mode is enabled.
10. ADDR DELAY — TSA signal used to indicate if the response address delay mode is enabled or disabled.
11. ADEL_CLKA — TSA timing module signal from TSA used to delay the memory address to the record memory.
12. PROBE STROBE — Selected signal that latches and records the probe data from the SR211 probe pod.
13. RMA — Record Memory Address. Refer to section 4.3.2
14. GOOD0- — Latched signal from the SR211 probe pod that indicates that the probe tip is in contact with a signal that is lower than the programmed input low reference.
15. GOOD1- — Latched signal from the SR211 probe pod that indicates that the probe tip is in contact with a signal that is higher than the programmed input high reference.
16. PGOOD0 — Signal from the SR211 probe pod that indicates that the probe tip is in contact with a signal that is lower than the programmed input low reference.
17. PGOOD1 — Signal from the SR211 probe pod that indicates that the probe tip is in contact with a signal that is higher than the programmed input high reference.

4.3.1 Strobe Select

The strobe select allows the user to select the PROBE STROBE and the delay value.

The falling edge of PROBE STROBE causes the data from the SR211 probe pod to be registered. The registered data is then stored in the probe memory. Refer to section 4.3.3 for a description of the probe memory.

4.3.2 Address Logic

Figure 4-5 illustrates the SR210 probe memory address logic.

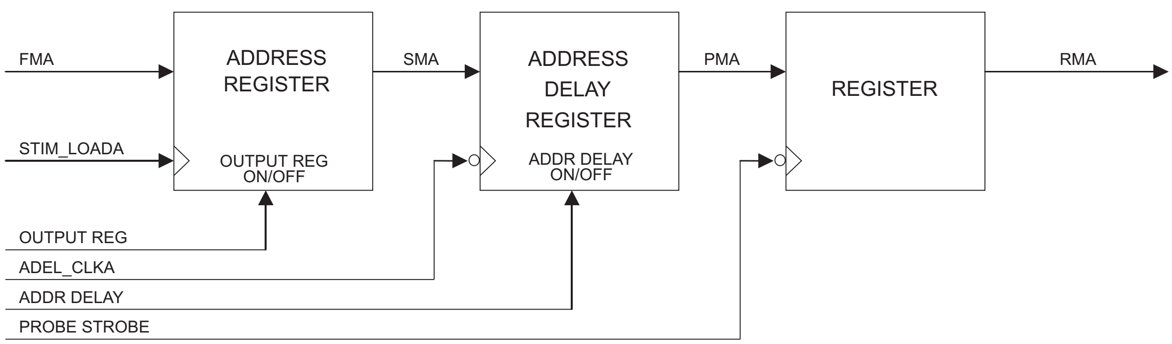


Figure 4-5 Input Address Logic Block Diagram

The following list describes the signals shown in figure 4-5 above.

1. FMA — Field Memory Address. This group of signals is generated by the TSA timing module. The FMA selects the stimulus/response memory word.
2. STIM_LOADA — TSA timing module signal that latches the stimulus address bus (FMA) when the output delay mode is enabled.
3. OUTPUT REG — Signal used to indicate if the output register mode is enabled or disabled.
4. ADEL_CLKA — TSA timing module signal used to delay the memory address to the record memory.
5. ADDR DELAY — Signal used to indicate if the response address delay mode is enabled or disabled.
6. PROBE STROBE — This signal latches data and generates the write pulse to the probe memory.
7. SMA — Stimulus Memory Address. Delayed FMA bus.
8. PMA — Present Memory Address. Delayed SMA bus.
9. RMA — Record Memory Address.

The address logic is used to delay the FMA bus to the probe memory.

As shown in figure 4-5 above there are two programmable delay blocks. The combination of these two programmable delays defines four input modes described in the following table 4-2.

Input Mode	Description	Required Timing Signals
Mode 1 (default)	Output register mode enabled and the input address delay mode disabled.	STIM_LOAD rising edge.
Mode 2	Both Output register mode and input address delay mode enabled	STIM_LOAD rising edge, ADEL_CLK falling edge.
Mode 3	Both output register mode and address delay mode disabled.	NA

Table 4-2 Addressing Mode Descriptions

These input modes are required in stimulus/response applications to keep the stimulus data synchronized with the response data.

4.3.3 Probe Memory

The probe memory on the SR210 consist of a 128K x 8 bit static RAM that stores the registered GOOD0 and GOOD1 data from the SR211 probe pod.

Table 4-1 below illustrates the probe memory results of the probe memory data.

GOOD0- (D7)	GOOD1- (D6)	Probe Result
0	0	Invalid code
0	1	Data at probe tip lower than programmed VIL.
1	0	Data at probe tip higher than programmed VIH.
1	1	Data at probe tip between the programmed VIH and VIL.

Table 4-1 Probe Memory Description

4.3.4 Input Register Logic

The input mode logic consists of a register for GOOD0 and GOOD1 probe signals registered by the selected strobe. The registered data is stored in the probe memory immediately after the selected strobe signal.

Appendix A Glossary of Terms

A16/A24/A32	VXI Register Based Programming Mode.
ADEL_CLK	Timing module signal from TSA used to delay the memory address to the probe memory.
ADDR DELAY	Signal used to indicate if the response address delay mode is enabled or disabled.
CELL	A cell is a single element of a timing set. A timing set can have from 2 to 256 cells. 1 CELL = 1 period of TS_CLK.
CLKA	Front panel SMA TTL clock sourced by PGMCLK1 from the SR210 clock generator.
CLKB	Front panel SMA TTL clock sourced by PGMCLK2 from the SR210 clock generator.
CLKC	Front panel SMA variable voltage clock sourced by PGMCLK2 from the SR210 clock generator.
FCNTL1	Front panel input signal (from the J8 connector) that can be selected to strobe probe data.
FCNTL2	Front panel input signal (from the J8 connector) that can be selected to strobe probe data.
FMA	Field Memory Address. This group of signals is generated by timing module TSA and broadcast to the I/O modules. The FMA generates the probe memory word.
FUNCTION CODE(FC)	Each module in a SR192 is assigned a 256K segment of the A32/A24 address map. The 256K can be split into sixteen unique areas via an additional four bits (F0-F3) which is routed to each module. The binary weighted value of the four signals generates sixteen function codes. Each module can define a single register for each function code or an array of 256K registers. Appendix B lists the function codes for this module.
GOOD0	Signal from the SR211 probe pod that flags a voltage at the SR211 probe tip that is less than the VIL reference.
GOOD1	Signal from the SR211 probe pod that flags a voltage at the SR211 probe tip that is greater than the VIH reference.
PROBE STROBE	This signal records data into the probe register, initiates the real time compare, latches the PMA bus and finally generates the write pulse to the record memory.
OUTPUT REG	Signal used to indicate if the output register mode is enabled or disabled.
SEQUENCE	A sequence is the link between the timing sets and the tables.
STIM_LOAD	Timing module control signal from TSA that latches the FMA address when the output register mode is enabled.
SUBSEQUENCE	A subsequence is a single element of a sequence. A subsequence selects a timing set, table, loop count, jump condition and control flags.

TABLE	A table is the structure that defines a FMA range for the subsequence. The FMA range is broadcast to all the I/O modules connected to the timing module.
TIMING MODULE	Any of Talons Timing Modules for the SR192.
TIMING SET	A timing set is the structure that is created that defines the stimulus/response timing. Four pages of sixteen timing sets can be defined.
TRANSFER	See WORD.
TSOUT5	Timing Set Output Five. General purpose output signal generated by the timing module. Also used as a strobe for the SR121/SR210 probe.
TSSTROBE1	Timing Set Strobe One. This signal, generated by the timing generator, can be selected to strobe the probe data.
TSSTROBE2	Timing Set Strobe Two. This signal, generated by the timing generator, can be selected to strobe the probe data.
VADDR	The address bus from the VXI Backplane.
VDATA	The data bus from the VXI Backplane.
VECTOR	See WORD.
VOH	Variable voltage output high reference.
VOL	Variable voltage output low reference.
VIH	Variable voltage input high reference.
VIL	Variable voltage input low reference.
WORD	A word is a single element of a table. The width of a word depends on the number and type of I/O modules installed in the SR192.

Appendix B Function Code Map

Address Location:

Accessory module located at hex address 0x70000.

Probe Memory located at hex address 0xC0000.

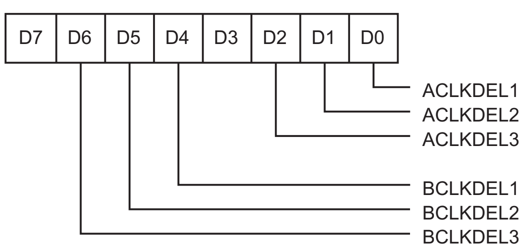
Specifications:

- Three modules make up the SR210. They are a programmable clock, a probe interface, and a DAC.
- Programmable Clock: Two channels (PGMCLK1 and PGMCLK2)
  100Hz-50MHz, .019Hz resolution.
  2ns jitter max.
  3 front panel signals:
  - CLKA = delayed PGMCLK1
  - CLKB = delayed PGMCLK2
  - CLKC = variable voltage PGMCLK2 (+/- 8V)
- Probe Interface: 128K GOOD0, GOOD1 memory.
  SR211 interface logic via J9 connector.
  Strobe Selections:
  - TSSTROBE1
  - TSSTROBE2
  - FCNTL1
  - FCNTL2
  - TSOUT5 (default)

  Strobe delay 0 to 28ns.
- DAC 18 programmable references (+15 to -15) auto calibrating.
  10mv resolution.

Function Code Assignments:

FC1 Write Clock Delay (word).
The clock delay for the SR210 Multifunction card is programmed by sending commands through this register. Bits 0, 1, and 2 are used to program the delay for clock A. Bits 4, 5, and 6 are used to program the delay for clock B.



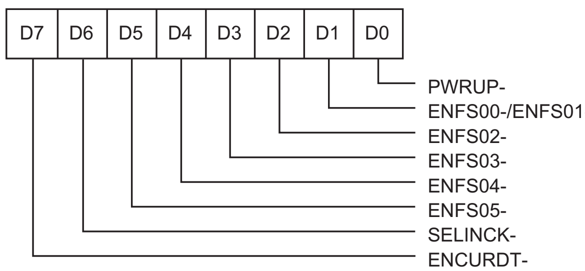
D2	D1	D0	CLKA Delay
0	0	0	0
0	0	1	5
0	1	0	10
0	1	1	15
1	0	0	20
1	0	1	25
1	1	0	30

1	1	1	35

D6	D5	D4	CLKB Delay
0	0	0	0
0	0	1	5
0	1	0	10
0	1	1	15
1	0	0	20
1	0	1	25
1	1	0	30
1	1	1	35

FC2 Write Clear Drive Fault (word).
This decode resets the latched drive fault signal generated by CLKC (programmable clock, SMAPCLK).

FC3 Write Enable Clock Drivers (word).
The commands sent to bits 0 through 6 in this register enable the drivers used for the clocks available on the SR210 Multifunction card. Bit 7 enables the over current detect logic.



PWRUP-	Enables the CLKC output (1 - ON, 0 - OFF)
ENFS00-ENFS01-	Timing Module PGMCLK source select. (1 - PGMCLK1, 0 - PGMCLK2)
ENFS02-	Unused clock output (1 - ON, 0 - OFF)
ENFS03-	Enables the CLKB output (1 - ON, 0 - OFF)
ENFS04-	Unused clock output (1 - ON, 0 - OFF)
ENFS05-	Enables the CLKA output (1 - ON, 0 - OFF)
SELINCK-	125MHz clock source for frequency synthesizers. (1 - Internal, 0 - External)
ENCURDT-	Enables the current detect logic on SMAPCLK circuit. (0 - ON, 1 - OFF)

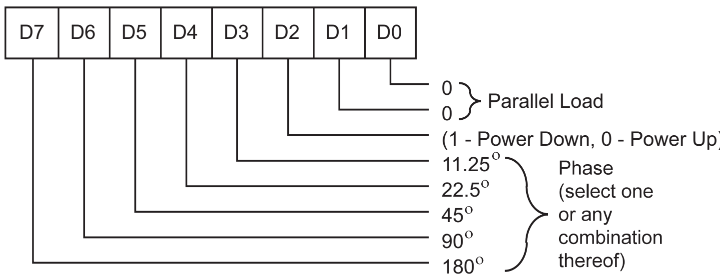
FC4 Read/Write Programmable Clock 1, PGMCLK1 (word).
Writes to this register program the frequency tuning, control, and phase modulation of the AD9850 clock generator that is connected to PGMCLK1. Reads from this register generates a frequency update signal (UPDATE0+).

The clock generator is programmed by sending five bytes described below:

Byte	D7	D6	D5	D4	D3	D2	D1	D0
0	Phase-b4 (MSB)	Phase-b3	Phase-b2	Phase-b1	Phase-b0	Power-Down	Control	Control
1	Freq-b31 (MSB)	Freq-b30	Freq-b29	Freq-b28	Freq-b27	Freq-b26	Freq-b25	Freq-b24
2	Freq-b23	Freq-b22	Freq-b21	Freq-b20	Freq-b19	Freq-b18	Freq-b17	Freq-b16
3	Freq-b15	Freq-b14	Freq-b13	Freq-b12	Freq-b11	Freq-b10	Freq-b9	Freq-b8
4	Freq-b7	Freq-b6	Freq-b5	Freq-b4	Freq-b3	Freq-b2	Freq-b1	Freq-b0

The first byte determines phase modulation, power-down enable, and loading format. The last four bytes determine the 32-bit frequency tuning word used by the AD9850's direct digital synthesizer.

The following figure describes word 0:



Bytes 1 through 5 are calculated using the following formula:

$F_{word} = F_{hz} / (125000000 / 2^{32})$

Where F_{word} = 32 bit tuning word and F_{hz} = desired clock frequency in hertz.

For example if the user wants 5.16MHz then:

F_{word} = 5160000 / 0.0291038304567 = 177296249.9 = $A91537A_{16}$

Byte 0 = 0 (default if F_{word} is not zero, 4 otherwise)

Byte 1 = 0

Byte 2 = $A9_{16}$

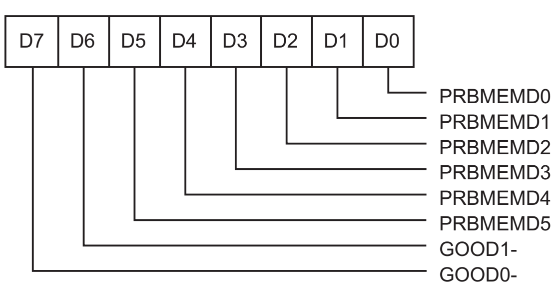
Byte 3 = 15_{16}

Byte 4 = 37_{16}

Before byte 0 and after byte 5 generate an update signal. The update before byte 0 resets the AD9850s byte counter to 0. The update after byte 5 programs the new frequency tuning word.

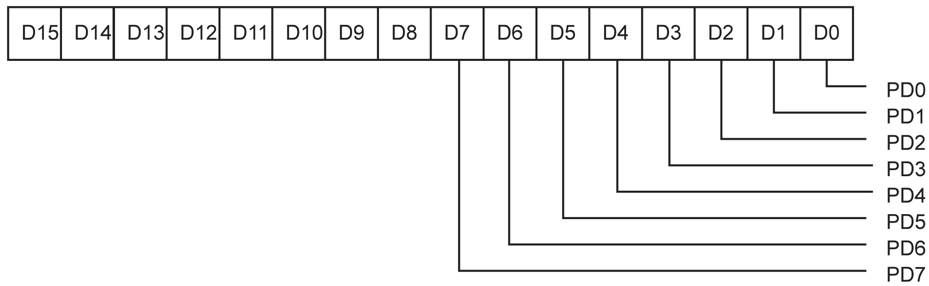
FC5 Read/Write Programmable Clock 2, PGMCLK2 (word).
Writes to this register program the frequency tuning, control, and phase modulation of the AD9850 clock generator that is connected to PGMCLK2. Reads from this register generates a frequency update signal (UPDATE0+). See FC4 for description and example.

FC6 Read/Write GOOD0/GOOD1 memory at address hex C0000 (byte/word).
The probe portion of the SR210 Multifunction card contains a single 128K x 8 bit static RAM for storing the results from the SR211 Pod.



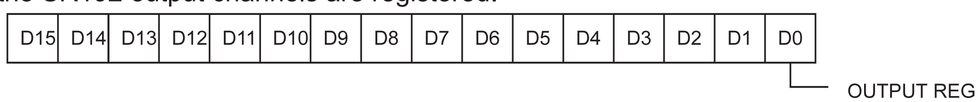
FC7 Read/Write SR211 pod data (word).
The SR211 probe pod is programmed by sending commands through this register.

The lower 8 bits contain the command/response data.



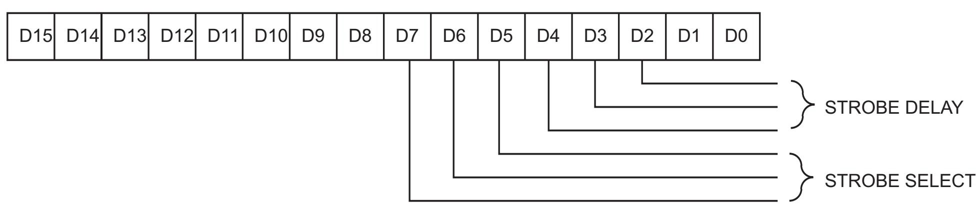
Refer to the SR211 probe manual for a description of the command/response data.

FC8 Write Output Register Delay Mode.
The output register delay is used to compensate the record address when the SR192 output channels are registered.



OUTPUT REG Enables/disables the output register address delay.
(0 - disable, 1 - enable)

FC9 Write Probe Strobe Selection/Delay.
The signal used to record the GOOD0 and GOOD1 signal from the SR211 Pod is selected by this function code.



D4	D3	D2	Strobe Delay
0	0	0	0
0	0	1	5
0	1	0	10
0	1	1	15
1	0	0	20
1	0	1	25
1	1	0	30
1	1	1	35

D7	D6	D5	Strobe Select
0	0	0	TSSTROBE1
0	0	1	TSSTROBE2
0	1	0	FCNTL1
0	1	1	FCNTL2
1	0	0	TSOUT5
1	0	1	PROBEDAT
1	1	0	X
1	1	1	X

FCA Write Address Delay Mode.

The address delay mode is used to compensate the record address when the response data is valid after the next stimulus is being output.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D0: ADDR DELAY

ADDR DELAY	Enables/disables the address delay. (0 - disable, 1 - enable)

FCC Read/Write Voltage References.

Commands sent to this register program the reference voltages for driver/receiver modules.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D0: CS-
D1: CLK-
D2: DIN

CS-	Chip Select signal to the PIC.
CLK-	Serial data clock to the PIC.
DIN	Serial data input to PIC.

Programming the reference voltages is performed by writing three bytes to the PIC controller that maintains the reference voltages using phase width modulation (PWM). The three bytes are described below:

Byte	Data
0	Reference
1	Voltage (MSB)
2	Voltage (LSB)

Byte 0 determines which one of the 17 reference to program:

0 VOL1
1 VOH1
2 VIL1
3 VIH1
4 VOL2
5 VOH2
6 VIL2
7 VIH2
8 VOL3
9 VOH3
10 VIL3
11 VIH3
12 VISR1
13 VISR2
14 VISR3
15 VISRCLK
16 VOLCLK
17 VOHCLK

Byte 1 and Byte 2 These two bytes form a 16 bit voltage word.

Byte 1 and 2 are calculated using the following formula:

$V_{word} = V / 0.01$

Where V_{word} = 16 bit voltage word and V = desired reference voltage in volts.

For example if the user wants VIH2 = 3.25V then:

$V_{word} = 3.25 / 0.01 = 325 = 145_{16}$

Byte 0 = 7

Byte 1 = 1

Byte 2 = 45_{16}

The 3 data bytes are sent msb to lsb with a delay of at least 15ms between bytes.

The following describes the DAC programming sequence:

Set CS- low, CLK- high

For (data = msb to lsb of byte 0)

Set DIN = data

Set CLK- low

Set CLK- high

Delay 15ms

For (data = msb to lsb of byte 1)

Set DIN = data

Set CLK- low

Set CLK- high

Delay 15ms

For (data = msb to lsb of byte 2)

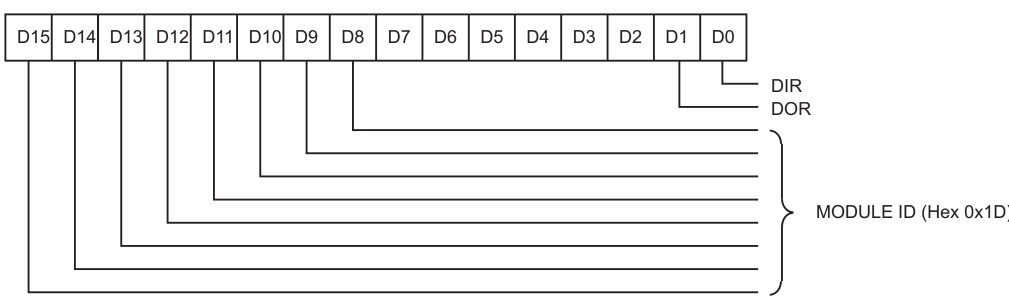
Set DIN = data

Set CLK- low

Set CLK- high

Set CS- high

FCF Read status/ID.
The status/ID register is unique for each module and is described below.



DIR	low - SR211 pod Ready for next command, high - Ready for next parameter.
DOR	low - SR211 pod Output data not ready, high - Output data ready.

Appendix C Programming Examples

The following examples illustrate the SR210 operation.

Refer to the SR192 Operators Manual for a complete description of the SCPI commands and parameter conventions.

Refer to the SR192 Plug & Play help file for a complete description of instrument drivers, parameters and conventions.

1 Clock

The following sections describe the SCPI commands and VXI Plug & Play instrument driver programming examples for the SR210 clock generator.

1.1 Setting the Reference Clock Source

The following sections illustrate the SCPI and Plug & Play functions used to select the programmable clock reference source.

1.1.1 SCPI Command

OUTPut:PGMClk1:REFerence <source>

Parameter Description:

<source>	Desired reference source. Range: INTernal, EXTernal.

Examples:

OUTP:PGMCLK1:REF INTERNAL	Sets clock generator reference to internal..
OUTPUT:PGMC1:REF?	Query returns "INT"

1.1.2 Plug & Play Driver

Function "tasr192_setFpClockRef" is used to program both PGMCLK1 and PGMCLK2 clock reference.

Examples:

```
/* Set the programmable clock reference to internal 125MHz */
tasr192_setFpClockRef (handle,
                TASR192_INT);            /* clock generator reference source */
```

1.2 Setting the Frequency

The following sections illustrate the SCPI and Plug & Play functions used to program the programmable clock frequency.

1.2.1 SCPI Command

OUTPut:PGMClk<1 | 2>[:DATA] <frequency>

Parameter Description:

<Frequency>	Desired clock frequency in Hz. Range: 100 to 50000000 (50e6).

Examples:

OUTP:PGMCLK1:DATA 13.33e3	Sets PGMCLK1 to 13.33KHz
OUTPUT:PGMC1?	Query returns "13330"
OUTPUT:PGMC2 50000000	Sets PGMCLK2 to 50MHz
OUTPUT:PGMCLK2:DATA?	Query returns "50000000"

1.2.2 Plug & Play Driver

Function “tasr192_setPgmclkFreq” is used to program both PGMCLK1 and PGMCLK2.

Examples:

```
/* Program PGMCLK1 to 13.33Khz and PGMCLK2 to 50MHz */
tasr192_setPgmclkFreq (handle,
                       13330,              /* PGMCLK1 frequency */
                       50e6);              /* PGMCLK2 frequency */
```

1.3 Assigning PGMCLK to Timing Module TS_CLK

The following sections illustrate the SCPI and Plug & Play functions used to assign PGMCLK1 or PGMCLK2 to the timing modules.

> **NOTE**
> **Both TSA and TSB timing modules are linked to the same PGMCLK selection, i.e., if TSA is assigned PGMCLK1 then TSB cannot select PGMCLK2 and vise versa.**

1.3.1 SCPI Command

TIMing:SETup:CLOCk <source>

Parameter Description:

<source>	TS_CLK source. Range: 10, 20, 50, EXTernal1, EXTernal2, PGMClk1, PGMClk2.

Examples:

MOD:SEL TSA	Selects TSA timing module
TIM:SET:CLOC PGMCLK1	Sets PGMCLK1 as TSA TS_CLK
TIMING:SETUP:CLOCK?	Query returns “PGMC1”

1.3.2 Plug & Play Driver

Function “tasr192_timingParameters” is used to program timing module parameters.

Examples:

```
/* Program PGMCLK1 as TSA TS_CLK source */
tasr192_timingParameters(handle,
                       TASR192_TSA,              /* timing module */
                       TASR192_CLK_PGMC1,        /* TS_CLK source */
                       0,                        /* timeout setting */
                       0,                        /* delay setting */
                       TASR192_TSIN2_LEVEL );    /* TSINPUT2 mode */
```

1.4 Programming the Front Panel Clocks (CLKA, CLKB and CLKC)

The following sections illustrate the SCPI and Plug & Play functions used to program the front panel clocks.

1.4.1 SCPI Commands

OUTPut:CLK<A | B>:DELay <delay value>

OUTPut:CLKC:REFerence:HIGH <voh>

OUTPut:CLKC:REFerence:LOW <vol>

OUTPut:CLK<A | B | C>[:STATE] <state>

Parameter Description:

<delay value>	CLKA or CLKB delay value where each delay is approximately 4ns.

	Range: 0 to 7.	
<voh>	CLKC output high.	
	Range: +8V to VOL	
<vol>	CLKC output low.	
	Range: VOH to -8V	
<state>	CLKA, CLKB or CLKC driver state.	
	Range: (ON | OFF | 1 | 0)	

Examples:

OUTP:CLKA:DELAY 4	Sets CLKA delay to 4.
OUTP:CLKB:DEL 7	Sets CLKB delay to 7.
OUTPUT:CLKC:REF:HIGH 3.5	Sets CLKC output high to 3.5V.
OUTPUT:CLKC:REF:LOW -0.5	Sets CLKC output low to -0.5V.
OUTP:CLKA ON	Turns CLKA on.
OUTP:CLKB:STATE 0	Turns CLKB off.
OUTPUT:CLKC:STAT 1	Turns CLKC on.

1.4.2 Plug & Play Driver

Function “tasr192_setFpClockParams” is used to program the CLKA/CLKB delay and CLKC levels.
Function “tasr192_setFpClockState” is used to enable/disable the front panel clock drivers.
Examples:

```
/* Program CLKA delay to 4 and CLKB to 7, CLKC voh = 3.5, CLKC vol - -0.5 */
tasr192_setFpClockParams(handle,
                    4,                      /* CLKA delay */
                    7,                      /* CLKB delay */
                    3.5,                    /* CLKC voh */
                    -0.5);                  /* CLKC vol */
/* Turn CLKA on, CLKB off and CLKC on */
tasr192_setFpClockState(handle,
                    TASR192_CLK_ON,         /* CLKA state */
                    TASR192_CLK_OFF         /* CLKB state */
                    TASR192_CLK_ON);        /* CLKC state */
```

1.5 Resetting CLKC Overdrive Fault

The following sections illustrate the SCPI and Plug & Play functions used to reset CLKC overdrive fault latch.

1.5.1 SCPI Commands

OUTPutPGMC1:RESet

Examples:

OUTP:PGMCLK1:RESET	Resets CLKC overdrive fault.

1.5.2 Plug & Play Driver

There is no Plug & Play drive for this function.
Use “tasr192_sendSingleCommand” to send the SCPI command above.

2 DAC

The following sections describe the SCPI commands and VXI Plug & Play instrument driver programming examples for the SR210 DAC.

2.1 Programming the References

The following sections illustrate the SCPI and Plug & Play functions used to program the DAC references.

2.1.1 SCPI Commands

OUTPut:REFerence:SELect <group>

OUTPut:REFerence:HIGH[:DATA] <voh>

OUTPut:REFerence:LOW[:DATA] <vol>

INPut:REFerence:SELect <group>

INPut:REFerence:HIGH[:DATA] <vih>

INPut:REFerence:LOW[:DATA] <vil>

Parameter Description:

<group>	SR210 voltage group. Range: VGRP1, VGRP2, VGRP3 or ALL.
<voh>	Output high. Range: +15V to VOL
<vol>	Output low. Range: VOH to -15V
<vih>	Input high. Range: +15V to VIL
<vil>	Input low. Range: VIH to -15V

Examples:

OUTP:REFERENCE:SEL VGRP1	Select voltage group one.
OUTP:REF:HIGH 7.5	Sets VOH1 to +7.5V.
OUTP:REF:LOW -2	Sets VOL1 to -2V.
OUTPUT:REF:ISR 3.5	Sets VISR1 to 3.5V.
INP:REFERENCE:SEL VGRP1	Select voltage group one.
INPUT:REF:HIGH 4.25	Sets VIH1 to 4.25V.
INP:REF:LOW 1.8	Sets VIL1 to 1.8V.

2.1.2 Plug & Play Driver

Function “tasr192_setOutputLevels” is used to program the CLKA/CLKB delay and CLKC levels.

Function “tasr192_setInputLevels” is used to enable/disable the front panel clock drivers.

Examples:

```
/* Program VOH1 to 7.5, VOL1 to -2 and VISR1 to 3.5 */
tasr192_setOutputLevels(handle,
        TASR192_VGRP1,      /* Voltage group */
        7.5,                /* VOH */
        -2,                 /* VOL */
        3.5);               /* VISR */
```

```
/* Program VIH1 to 4.25 and VIL1 to 1.8 */
tasr192_setInputLevels(handle,
                    TASR192_VGRP1,          /* Voltage group one */
                    4.25,                   /* VIH */
                    1.8);                   /* VIL */
```

3 Probe

The following sections describe the SCPI commands and VXI Plug & Play instrument driver programming examples for the SR210 Probe.

3.1 Programming The SR211 Probe Setup

The following sections illustrate the SCPI and Plug & Play functions used to program the SR211 pod setup settings.

3.1.1 SCPI Commands

INPut:PROBe:SWITch <switch>,<switch mode>
INPut:PROBe:REFerence:HIGH[:DATA] <vih>
INPut:PROBe:REFerence:LOW[:DATA] <vil>
INPut:PROBe:REFerence:LOGic <logic>
INPut:PROBe:MODE <mode>
INPut:PROBe:ORDelay <state>
INPut:PROBe:STRObe[:SOURce] <strobe>
INPut:PROBe:STRObe:DELay <delay>

Parameter Description:

<switch>	SR211 switch. Range: PROBE, S1 or S2
<switch mode>	Switch mode Range: AUTO, ACQuire or PULSe
<vih>	Probe input high. Range: +10V to -10V
<vil>	Probe input low. Range: +10V to -10V
<logic>	Logic family. Range: TTL (2.4, 0.8), ECL (-0.87, -1.475), LV (2.0, 0.8)
<mode>	Operating mode. Range: AUTO, MANual, ACQuire, PULSe, RESet
<state>	Output register delay state. Range: (ON | OFF | 1 | 0)
<strobe>	Probe strobe source. Range: TSOUT5, TSSTROBE1, TSSTROBE2, FCNTL1, FCNTL2
<delay>	Probe strobe delay. Range: 0 to 7

Examples:

INP:PROBE:SWITCH PROBE,ACQ	Set probe switch to initiate acquire mode.
INPUT:PROB:SWIT S1,AUTO	Set S1 switch to initiate auto mode.
INP:PROB:REF:LOG TTL	Sets probe reference vih to 2.4 and vil to 0.8.

INP:PROBE:MODE PULSE	Sets the SR211 mode to pulse detect.
INP:PROB:ORDELAY OFF	Sets probe output register delay mode off.
INP:PROB:STROBE TSSTROBE1	Sets probe strobe source to TSSTROBE1.
INP:PROB:STR:DELAY 0	Sets probe strobe delay to 0.

3.1.2 Plug & Play Driver

Function “tasr192_probeSetup” is used to program the probe reference and switch settings.
Function “tasr192_probeMode” is used to program the probe strobe mode.
Function “tasr192_probeOrdelay” is used to enable/disable the probe output register delay mode.
Function “tasr192_probeStrobe” is used to program the probe strobe source and delay.
Examples:

```
/* Program the probe references to TTL levels */
tasr192_probeSetup(handle,
            TASR192_PRB_TTL,        /* Probe reference setting */
            0,                      /* User defined vil */
            0,                      /* User defined vih */
            TASR192_PRB_ACQ,        /* Probe switch mode */
            TASR192_PRB_AUTO,       /* S1 switch mode */
            TASR192_PRB_NONE);      /* S2 switch mode */
/* Program probe mode as pulse detect */
tasr192_probeMode(handle,
            TASR192_PRB_PULS);      /* Probe mode setting */
/* Disable probe output register delay mode */
tasr192_probeOrdelay(handle,
            TASR192_ADLY_OFF); /* Probe mode setting */
/* Select TSSTROBE1 with a delay of zero as the probe strobe. */
tasr192_probeStrobe(handle,
            TASR192_PRB_TSST1,      /* Strobe source */
            0);                     /* Strobe delay */
```

3.2 Querying the SR211 Probe Data

The following sections illustrate the SCPI and Plug & Play functions used to query the SR211 probe data.

3.2.1 SCPI Commands

INPut:PROBe:STATus?
CALCulate:PCRC? <table>
Parameter Description:

<table>	SR192 table Range: NA	

Examples:

INP:PROBE:STAT? — Returns the following probe status:

Bit 0	GOOD0 Signal True(1)/False(0)
Bit 1	GOOD1 Signal True(1)/False(0)
Bit 2	TRISTATE Signal True(1)/False(0)
Bit 3	PULSE0 Signal True(1)/False(0)
Bit 4	PULSE1 Signal True(1)/False(0)

	Bit 5 OPEN Signal True(1)/False(0)
	Bit 6 NU
	Bit 7 NU
	Bit 8 PROBE switch True(1)/False(0)
	Bit 9 S1 switch True(1)/False(0)
	Bit 10 S2 switch True(1)/False(0)
	Bit 11 NU
	Bit 12 PROBE switch latched True(1)/False(0)
	Bit 13 S1 switch latched True(1)/False(0)
	Bit 14 S2 switch latched True(1)/False(0)
	Bit 15 NU
CALC:PCRC? DATA_IN	Returns the CRC generated from the GOOD0 Memory aligned with the table "DATA_IN".

3.2.2 Plug & Play Driver

Function "tasr192_queryProbeStatus" is used to program the probe reference and switch settings.
Function "tasr192_queryProbeCrc" is used to program the probe strobe mode.
Function "tasr192_queryProbeMemory" is used to query the probe memory.
Examples:

```
/* Get the probe status */
tasr192_queryProbeStatus(handle,
        &Status);                  /* Probe status variable */
/* Get the probe CRC for table "DATA_IN" */
tasr192_queryProbeCrc(handle,
        TASR192_TSA,               /* Timing module TSA */
        "DATA_IN",                 /* Alligned with table */
        &CRC);                     /* CRC variable */
/* Query probe memory */
tasr192_queryProbeMemory(handle,
        TASR192_TSA,               /* Timing module TSA */
        TASR192_TABLE,             /* Memory source */
        "DATA_IN",                 /* Alligned with table */
        0,                         /* NA, First memory address */
        0,                         /* NA, Size */
        Data_array);               /* ViChar array for probe data */
```