REFERENCE MANUAL

SR192A

192-Channel Modular
Digital Resource Module

Manual Revision: 04/09/06
Manual Part Number: SRRM122
Instrument Part Number: SR192A

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Follow these precautions:

- Don’t bypass the VXI chassis’ power cord’s ground lead with two-wire extension cords or plug adapters.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the VXI chassis power receptacle to the chassis ground terminal.
- Don't energize the VXI chassis until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and have instructions from Talon Instruments.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the **CAUTION** statements. They point out situations that can cause equipment damage.
- Use ESD static control procedures when handling the SR192A or any of its modules.

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1 Introduction

Talon's SR192A digital test module is a modular VXI stimulus/response system. The SR192A baseboard is a two slot, "C" size module which houses up to 12 I/O modules. I/O modules are designed to provide either 8 or 16 stimulus/response channels for a total of 96 or 192 channels. Modules provide many logic options such as fixed or variable voltage, single ended or differential. Some of the current I/O modules are listed below:

- SR125A - 16 channel single ended TTL.
- SR124A - 8 channel single ended TTL or differential RS485/422 per pin.
- SR126A - 8 channel differential LVDS.
- SR214A - 16 channel single ended variable voltage (+7V to -5V).

Multiple SR192A's may be linked in a master/slave configuration to provide up to 1152 channels in a single VXI 13-slot chassis.

The SR101A Timing Module provides all the timing and control for the SR192A I/O modules when executing a stimulus/response operation or emulating a bus interface. After being programmed and commanded to start, the SR101A can generate output signals to the UUT, test input signals from the UUT (i.e. Handshake or test input), generate memory address and control signals for the SR192A I/O modules, and finally test the results from the I/O modules.

Each SR192A may have one or two SR101A modules installed . The first is always installed into the TSA timing module slot and the second optionally installed into the TSB timing module slot. TSA controls up to six I/O modules, channels 1-96. TSB controls up to six I/O modules, channels 97-192. The Timing modules may operate independently or may be synchronized with one another. Additionally, Timing modules from different SR192A's may be synchronized together through the J7 master/slave front panel connector.

This manual is for the SR192A baseboard and its components.

1.1 Manual Layout

This manual contains technical information on the SR192A and all of its components.

The layout of this manual is in five sections described below:

1. Introduction	This section.
2. Specifications	Electrical and environmental specifications of the SR192A.
3. Jumpers/Installation	Description of the jumpers and installation of the SR192A.
4. Functional Description	Functional description of the SR192A hardware.

In addition, five appendices are included:

A. Glossary of Terms	Description of terms used in this manual.
B. Function Code Map	Hardware register description.

1.2 SR192A System

The SR192A system is comprised of the following components; front panel, baseboard, digital resource A and digital resource B as well as the following modules; TSIO and CPU/VXI. An optional multi function card (MFC) is available that adds clock and probe logic to the system.

1.2.1 Front Panel

The SR192A front panel provides the hardware interface to the UUT.

Section 4 of the SR192A Operators Manual lists the pinouts for the SR192A front panel connectors.

1.2.2 Baseboard

The baseboard PCB is a “C” sized VXI board which contains the connectors and headers required for routing signals to/from SR192A components.

1.2.3 Digital Resource A

Digital resource A is comprised of the following module slots on the baseboard:

TSA	Timing module slot that generates the address and control signals for the I/O modules installed in slots DRA1 through DRA6.
DRA1	I/O module slot that contains the driver, receivers and memory for the front panel channels 1 through 16.
DRA2	I/O module slot that contains the driver, receivers and memory for the front panel channels 17 through 32.
DRA3	I/O module slot that contains the driver, receivers and memory for the front panel channels 33 through 48.
DRA4	I/O module slot that contains the driver, receivers and memory for the front panel channels 49 through 64.
DRA5	I/O module slot that contains the driver, receivers and memory for the front panel channels 65 through 80.
DRA6	I/O module slot that contains the driver, receivers and memory for the front panel channels 81 through 96.

1.2.4 Digital Resource B

Digital resource B is comprised of the following module slots on the baseboard:

TSB	Timing module slot that generates the address and control signals for the I/O modules installed in slots DRB1 through DRB6.
DRB1	I/O module slot that contains the driver, receivers and memory for the front panel channels 97 through 112.
DRB2	I/O module slot that contains the driver, receivers and memory for the front panel channels 113 through 128.
DRB3	I/O module slot that contains the driver, receivers and memory for the front panel channels 129 through 144.
DRB4	I/O module slot that contains the driver, receivers and memory for the front panel channels 145 through 160.
DRB5	I/O module slot that contains the driver, receivers and memory for the front panel channels 161 through 176.
DRB6	I/O module slot that contains the driver, receivers and memory for the front panel channels 177 through 192.

1.2.5 TSIO Module

The TSIO module is an L shaped assembly which is installed in the P35 connector of the baseboard. This board is used to translate timing set signals TSOUTA1, TSOUTA2, TSINPA1, TSINPA2, CLOCKA, EXCLK1 and FCNTL1 to/from various logic families that are compatible with Talon’s family of I/O modules.

1.2.6 CPU/VXI Modules

The CPU module resides in the last slot of the baseboard and communicates with the VXI backplane through the VXI module. It contains a Motorola 68HC000 microprocessor, FLASHRAM, system RAM, VXI interface logic and SR192A address map decoding logic. The CPU provides a SCPI format compatible parser to control data flow to/from the VXI controller and communication registers for the VXI protocol requirements. The SR192A functions are programmed through VXI A32/A24 register access.

The FLASHRAM contains the SR192A operating system. Used in tandem with static memory it allows the operating system to be field upgradeable without hardware modification.

The CPU communicates with the various modules via the address and data bus of the SR192A baseboard. The upper addresses form a module decode for each module slot. Along with the module decodes each slot has four function code lines F0 through F3. These function code lines enable each module to define 16 unique function codes. These codes are used to pass module ID, operating status and commands to/from the CPU or VXI bus.

The VXI module is a small daughter board which mates with the CPU module and connects to the VXI system backplane . This module is the link to the SR192A for all VXI communication. In addition to providing the hardware link to the VXI bus, it houses the system RAM for downloading operating system changes to the CPU FLASHRAM.

1.2.7 MFC Module

The MFC module provides the following support logic for the SR192A system:

1. Interface logic for the SR211 Probe Pod.
2. User programmable clocks routed to the digital resources and front panel

2 Specifications

The following sections list the specifications of the SR192A module.

2.1 SR192A Baseboard

Number of digital I/O module slots 12
DRA1, DRA2, DRA3, DRA4, DRA5, DRA6, DRB1, DRB2, DRB3, DRB4, DRB5, DRB6
Number of timing module slots 2
TSA, TSB
Number of timing module I/O slots 1
TSIO
Number of accessory module slots 1
MFC
VXI Bus
Message Based
A16/D16 Slave
A24/A32 Required Memory[1] 8M
IEEE-488.2 Instrument (I4)
Event Generation (EG)
Interrupter
Static/Dynamic Configuration[1]
TTLTRG Drive TSOUT3A
Digital I/O Slot Signals
Maximum number of I/O channels 192
I/O channel Termination .....See specific I/O module manual
Memory depth per I/O channel .....See specific I/O module manual
Number of control channels.....See specific I/O module manual
Control channel Termination .....See specific I/O module manual
Timing Slot Signals
Number of output trigger, handshake lines (TSOUT1-TSOUT5, SYNC PULSE).....6 per slot
Output trigger, handshake termination[2] .....See section 3.6
Number of input trigger, handshake lines (TSINPUT1,TSINPUT2).....2 per slot
Input trigger, handshake termination[3] .....See section 3.6
External I/O control inputs (FCNTL1, FCNTL2)[4] 2
External I/O control input termination[4] .....See section 3.6
External clock inputs (EXCLK1, EXCLK2)[5] 2
External clock input termination[2] .....See section 3.6
Selected clock output (CLOCKA[6], CLKOUTA, CLOCKB, CLKOUTB) .....2 per slot
Selected clock output termination[6] .....See section 3.6
Busy flag output (TSABUSY, TSBBUSY).....1 per slot
Busy flag output termination .....None
MFC Accessory Module Signals .....See specific accessory module manual
VXI Backplane Signals
Output Low Sink Current (TTLTRG0 - TTLTRG7, IRQ1 - IRQ7) .....24 mA

Note 1: Switch Selection
Note 2: TSOUTA1 and TSOUTA2 routed through TSIO, see section 3.4 and 4.7.1
Note 3: TSINPUTA1 and TSINPUTA2 routed through TSIO, see section 3.4 and 4.7.2
Note 4: FCNTL1 routed through TSIO, see section 3.4, 4.6, and 4.9
Note 5: EXCLK1 routed through TSIO, see section 3.4 and 4.5
Note 6: CLOCKA routed through TSIO, see section 3.4 and 4.5

2.2 Electrical

The following lists the electrical characteristics of the SR192A baseboard driver/receivers

TTL Signals
High Level Output Voltage .....2.4V min
High Level Source Current.....15 mA
Low Level Output Voltage .....0.4V max
Low Level Sink Current.....25 mA
Output Impedance (with 47Ω series terminator).....80Ω typ
Short Circuit Protected.....Yes[1]
High Input Threshold.....2.0V min
Low Input Threshold.....0.8V max
Input Impedance .....None

The following lists the electrical characteristics of the SR192A TSIO driver/receivers

TTL Signals
High Level Output Voltage .....2.4V min
High Level Source Current.....15 mA
Low Level Output Voltage .....0.4V max
Low Level Sink Current.....25 mA
Output Impedance (with 47Ω series terminator).....80Ω typ

Short Circuit Protected.....Yes[1]
High Input Threshold.....2.0V min
Low Input Threshold.....0.8V max
Input Impedance (Variable Voltage TSIO, V+/V- Applied).....> 10KΩ
Input Impedance (Variable Voltage TSIO, V+/V- Not Applied).....900Ω @ 3V typ
Input Impedance (Differential TSIO).....82Ω typ

RS-422 Differential Signals

Differential Driver Output Voltage (Unloaded).....5V max
Differential Driver Output Voltage (Loaded 27 ohm, RS-485).....1.5V min
Differential Driver Output Voltage (Loaded 50 ohm, RS-422).....2V min
Differential Receiver Threshold.....-2V min, +2V max
Differential Receiver Hysteresis.....70mV typ
Differential Receiver common mode range.....-7V to +12V
Input/Output Impedance.....120Ω

Note 1: With 47Ω series terminator installed.

2.3 Timing Characteristics

The SR192A baseboard is one part of a modular system. Refer to the SR192A Timing Reference Manual for the timing characteristics of the SR192A system.

2.4 Environmental

Temperature Range

Operating .....0° C to +50° C
Storage .....-40° C to +70° C (RH not controlled)

Altitude

Operating .....Sea level to 10,000 ft.
Storage .....Sea level to 40,000 ft.

Relative Humidity (non condensing)

0°C to +10°C.....not controlled
+11°C to +30°C.....95+/-5%RH
+31°C to +40°C.....75+/-5%RH
+41°C to +50°C.....45+/-5%RH

2.5 Size

Dimension

Dual slot, “C” size VXI module. Approx. 26.22 cm x 6.09cm x 36.63 cm (10.325” x 2.4” x 14.42”)

Weight

< 1.81kg (4.0 lbs.)

2.6 Power Requirements

The power requirements listed in table 2-1 are for the SR192A baseboard with a TSIO, CPU and VXI modules.

Voltage	Peak Current	Dynamic Current	Note
+5V	1.36A	100mA	-
-5.2V	0	0	-
-2V	0	0	-
+12V	2mA	N/A	-
-12V	0	0	-
+24V	40mA	0	-
-24V	40mA	0	-
V+	200mA	100mA	1
V-	200mA	100mA	1

Note 1: Variable voltage TSIO only.

Table 2-1 Backplane Power Requirements

The following lists the front panel J10 V1+ and V1- voltage requirements with any variable voltage I/O modules installed in any DRA<n> slot.

V1+ maximum .....+11.5V
V1+ minimum .....+9.5V
V1+ nominal .....+10V
V1- maximum .....-7.5V
V1- minimum .....-8.5V
V1- nominal .....-8V

The following lists the front panel J10 V2+ and V2- voltage requirements with any variable voltage I/O modules installed in DRB1, DRB2 or DRB3 slot.

V2+ maximum .....+11.5V
V2+ minimum .....+9.5V
V2+ nominal .....+10V
V2- maximum .....-7.5V
V2- minimum .....-8.5V
V2- nominal .....-8V

The following lists the front panel J10 V3+ and V3- voltage requirements with any variable voltage I/O modules installed in DRB4, DRB5 or DRB6 slot.

V3+ maximum .....+11.5V
V3+ minimum .....+9.5V
V3+ nominal .....+10V
V3- maximum .....-7.5V
V3- minimum .....-8.5V
V3- nominal .....-8V

2.7 Cooling Requirements

The cooling requirements for an SR192A system requires that the total power used by the system must first be calculated (refer to Appendix C of the Operators Manual).

3 Jumpers/Installation

The following sections describe the jumpers and installation procedure for the SR192A including the CPU, VXI and TSIO modules.

3.1 Baseboard Jumpers, Test Points, Fuses and SW1

Figure 3-1 below is a locator diagram for test points, jumpers, fuses and SW1 located on the SR192A baseboard.

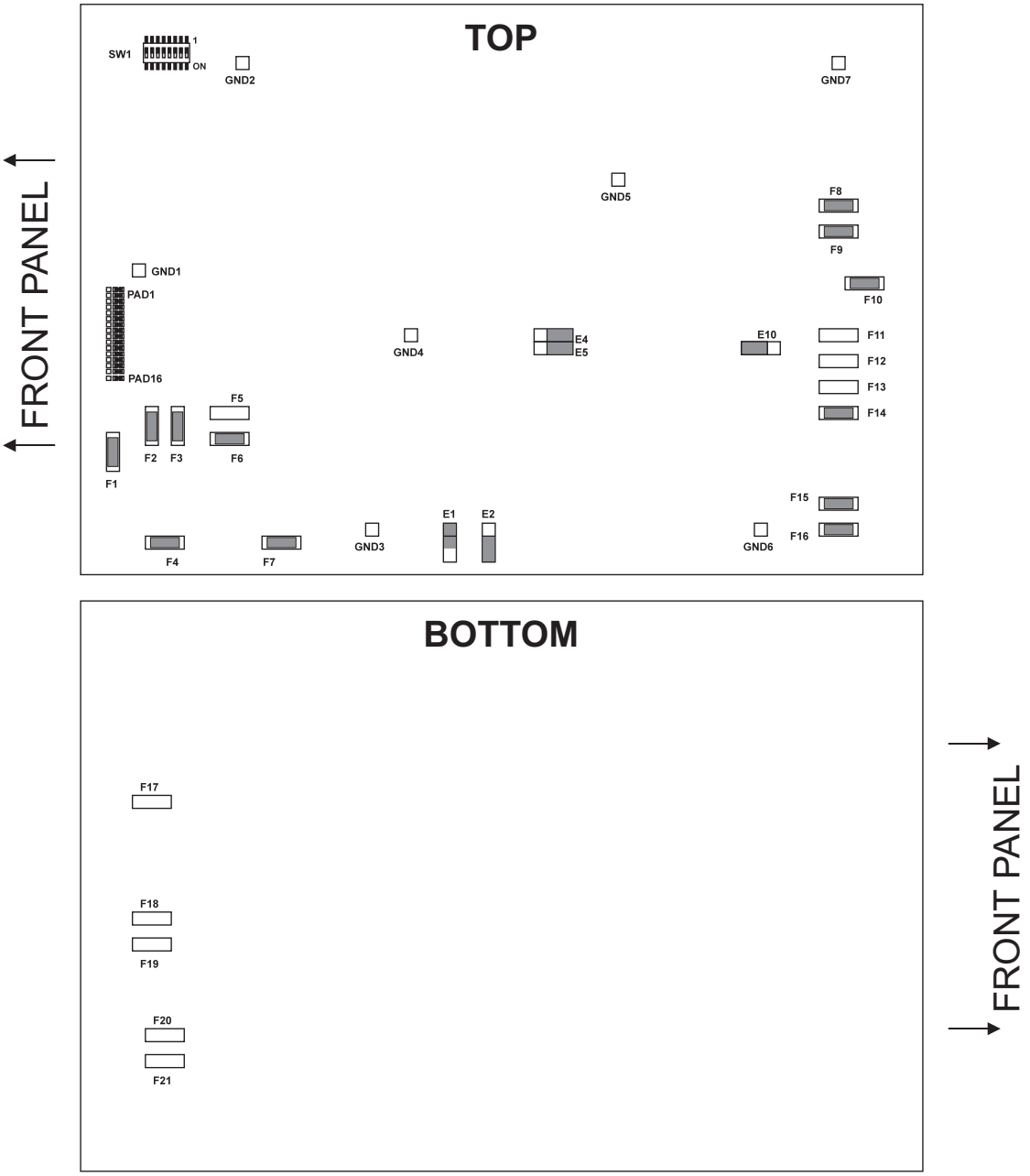

Figure 3-1 SR192A Baseboard Test Points, Jumpers, Fuses and SW1 Location

3.1.1 Baseboard Test Point Description

Table 3-1 describes the test points on the SR192A baseboard.

Mnemonic	Description
GND1	Signal ground
GND2	Signal ground
GND3	Signal ground
GND4	Signal ground
GND5	Signal ground
GND6	Signal ground
GND7	Signal ground

Table 3-1 SR192A Baseboard Test Point Description

3.1.2 Baseboard Jumper Description

The following sections describe the baseboard jumper options.

3.1.2.1 Probe/Reference Select (PAD1 through PAD16)

This set of sixteen jumper pads routes either the DAC reference or the SR211 probe control signals to the J9 front panel connector. The DAC references are selected by installing a zero ohm resistor between the two pads closer to the front panel. The SR211 Probe is selected (factory default) by installing a zero ohm resistor between the two pads furthest from the front panel. See figure 3-2 below.

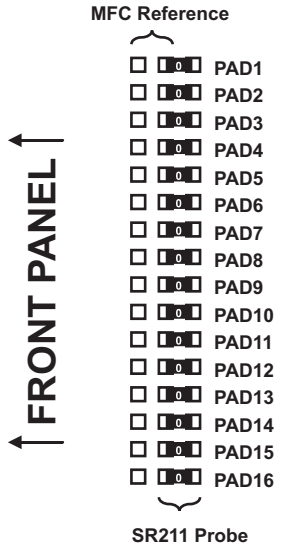

Figure 3-2 SR192A Baseboard J9 SR211/DAC Selection

3.1.2.2 TSINPUTMB Handshake Source (E1)

This jumper block selects the source for the TSINPUTMB handshake signal. Pin 1 to Pin 2 (factory default) connects the synchronized TSINPUT1A signal, pin 2 to pin 3 connects the buffered J7 TSINPUTM signal.

The pin 2 to pin 3 setting would only be used in all units of a multiple SR192A master/slave configured system.

3.1.2.3 TSA Input2 Handshake Source (E2)

This jumper block selects the source for the TSA input2 signal. Pin 2 to Pin 3 (factory default) connects the front panel buffered TSINPUT2A signal, pin 1 to pin 2 connects the selected TTLTRG signal from the VXI backplane. See TTLTRG- register in appendix B.

The pin 1 to pin 2 setting would only be used to trigger TSA using the VXI backplane.

WARNING

A trace may be present (factory default) that connects pin 2 to pin 3 and must be cut prior to connecting pins 1 and 2.

3.1.2.4 DRB4 Voltage Group Select (E4,E5)

These jumper blocks selects the voltage group for the DRB4 module. Pin 2 to pin 3 on all jumpers (factory default) connects DRB4 to voltage group 3, pin 1 to pin 2 connects voltage group 2.

Each voltage group is made up of two signals listed below along with the jumper that selects it:

Jumper (Signal)	DRB4 Slot Voltage Group	
	Pin 1 to Pin 2	Pin 2 to Pin 3 (Factory Default)
E4 (V+)	VGRP2 (V2+)	VGRP3 (V3+)
E5 (V-)	VGRP2 (V2-)	VGRP3 (V3-)

3.1.2.5 TSB Input2 Handshake Source (E10)

This jumper block selects the source for the TSB input2 signal. Pin 2 to Pin 3 (factory default) connects the front panel buffered TSINPUT2B signal, pin 1 to pin 2 connects the selected TTLTRG signal from the VXI backplane. See TTLTRG- register in appendix B.

The pin 1 to pin 2 setting would only be used to trigger TSB using the VXI backplane.

WARNING

A trace may be present (factory default) that connects pin 2 to pin 3 and must be cut prior to connecting pins 1 and 2.

3.1.2.6 V1+ Source Select (F1, F17)

The V1+ source is selected by installing one of two fuses. F1-7A installed (factory default) connects V1+ to the front panel J10 connector, F17 (2A max) installed connects V1+ to the VXI backplane +12V.

3.1.2.7 V1- Source Select (F5, F6, F13)

The V1- source is selected by installing one of three fuses. F6-7A installed (factory default) connects V1- to the front panel J10 connector, F5 (2A max) installed connects V1- to the VXI backplane -12V, F13 (7A max) installed connects V1- to VXI backplane -5.2V.

3.1.2.8 V2+ Source Select (F4, F18)

The V2+ source is selected by installing one of two fuses. F4-7A installed (factory default) connects V2+ to the front panel J10 connector, F18 (2A max) installed connects V2+ to the VXI backplane +12V.

3.1.2.9 V2- Source Select (F2, F12, F21)

The V2- source is selected by installing one of three fuses. F2-7A installed (factory default) connects V2- to the front panel J10 connector, F21 (2A max) installed connects V1- to the VXI backplane -12V, F12 (7A max) installed connects V2- to VXI backplane -5.2V.

3.1.2.10 V3+ Source Select (F7, F19)

The V3+ source is selected by installing one of two fuses. F7-7A installed (factory default) connects V3+ to the front panel J10 connector, F19 (2A max) installed connects V3+ to the VXI backplane +12V.

3.1.2.11 V3- Source Select (F3, F11, F20)

The V3- source is selected by installing one of three fuses. F3-7A installed (factory default) connects V3- to the front panel J10 connector, F20 (2A max) installed connects V3- to the VXI backplane -12V, F11 (7A max) installed connects V3- to VXI backplane -5.2V.

3.1.3 Baseboard Fuse Description

Table 3-2 describes the fuses on the baseboard for VXI backplane voltages used by the SR192A.

Fuse	Signal, Amps
F8	+12V, 2A
F9	-12V, 2A
F10	+5V, 15A
F14	-5.2V, 15A
F15	+24V, 2A
F16	-24V, 2A

Table 3-2 SR192A Baseboard Fuse Description

3.1.4 Baseboard SW1 Description

SW1 is used to terminate or pull-up the front panel J7 signals. All switches on (factory default) connects the termination and pull-up resistors to the front panel J7 connector, all switches off isolates the termination and pull-up resisters from the J7 connector.

SW1 is used in a master/slave SR192A system. All SR192A's in the chassis except for the last SR192A slave should set all SW1 switches off.

3.2 CPU Jumpers, Test Points and Switches

Figure 3-3 below is a locator diagram for test points, jumpers and switches located on the SR192A CPU module, part number 10510.

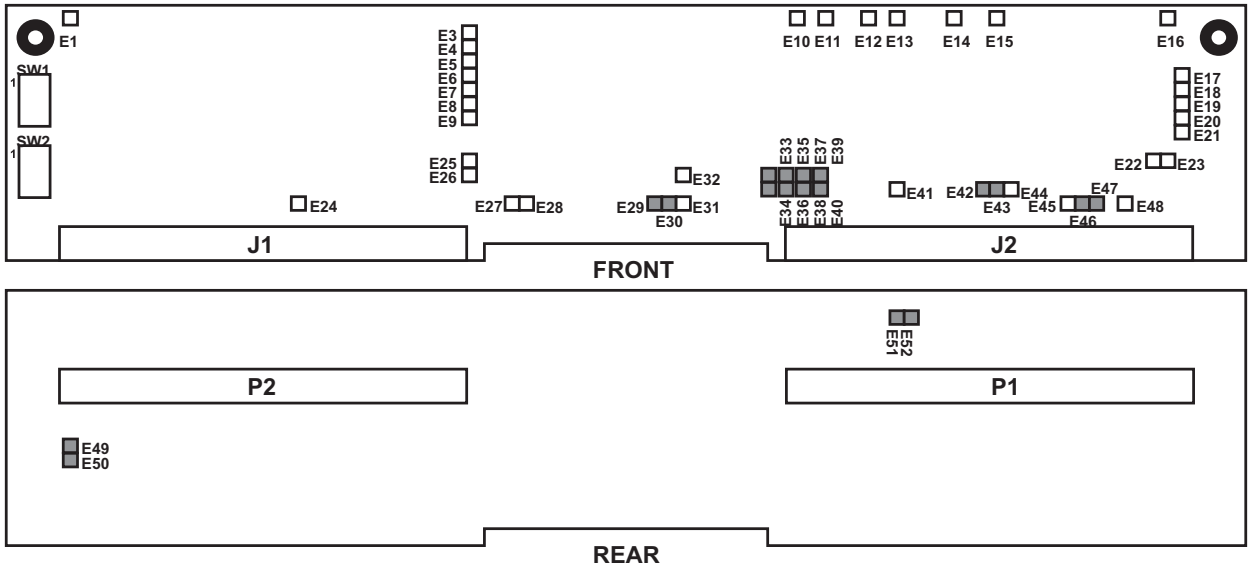

Figure 3-3 SR192A CPU Module Test Points, Jumpers and Switch Location

3.2.1 CPU Test Point Description

Table 3-3 describes the test points on the SR192A CPU module.

Mnemonic	Description
E1	Signal ground
E2	Signal ground
E3	+5V
E4	Signal Ground
E5	CCLK1
E6	DONE1
E7	DIN1
E8	PROG1
E9	LA19/INIT-
E10	UAS-
E11	CPU-
E12	Signal ground
E13	+5V
E14	Signal ground
E15	VXI-
E16	Signal ground
E17	+5V
E18	Signal Ground
E19	CCLK2
E20	DONE2
E21	DIN2
E22	PROG2-
E23	Signal Ground
E24	BS8-
E25	PROG1-
E26	Signal Ground
E27	UIPL2-
E28	UIPL1-
E32	UIPL0-
E41	GALIO1
E48	VAS-

Table 3-3 SR192A CPU Test Point Description

3.2.2 CPU Jumper Description

The following sections describe the CPU module jumper options.

3.2.2.1 U21 FPGA Cable Load (E42,E43,E44; E45,E46,E47; E49,E50)

U21 can be programmed through either a serial PROM or by a cable download. E42 connected to E43, E46 connected to E47 and E49 connected to E50 enables U21 to be loaded by the serial PROM (factory default). E43 connected to E44, E45 connected to E46 and E49 disconnected from E50 enables U21 to be loaded from the cable.

These jumpers are factory reserved and should not be modified.

WARNING

A trace may be present (factory default) that connects E49 to E50.

3.2.2.2 U6 FPGA Cable Load (E29,E30,E31; E51,E52)

U6 can be programmed through either a serial PROM or by a cable download. E30 connected to E31 and E51 connected to E52 enables U6 to be loaded by the serial PROM (factory default). E29 connected to E30 and E51 disconnected from E52 enables U6 to be loaded from the cable.

These jumpers are factory reserved and should not be modified.

WARNING

A trace may be present (factory default) that connects E51 to E52.

3.2.2.3 General Purpose SRIO (E33,E34; E35,E36)

Two general purpose I/O signals (SRIO1 and SRIO2) can be isolated from the SR192A baseboard. E33 connected to E34 and E35 connected to E36 connects the SRIO signals to the baseboard (factory default). E33 disconnected from E34 and E35 disconnected from E36 isolates the SRIO signals.

These jumpers are factory reserved and should not be modified.

3.2.2.4 CPWAIT Signal (E37,E38)

The CPWAIT signal can be isolated from the SR192A baseboard. E37 connected to E38 connects the CPWAIT signal to the SR192A baseboard (factory default). E37 disconnected from E38 isolates CPWAIT from the SR192A baseboard.

These jumpers are factory reserved and should not be modified.

3.2.2.5 UUTRST Signal (E39,E40)

The UUTRST signal can be isolated from the SR192A baseboard. E39 connected to E40 connects the UUTRST signal to the SR192A baseboard (factory default). E39 disconnected from E40 isolates UUTRST from the SR192A baseboard.

These jumpers are factory reserved and should not be modified.

3.2.3 CPU Switch Description

The following sections describe the CPU module switches.

3.2.3.1 Logical Address Switch Selection (SW1)

The following figure 3-4 below shows a logical address setting of 2.

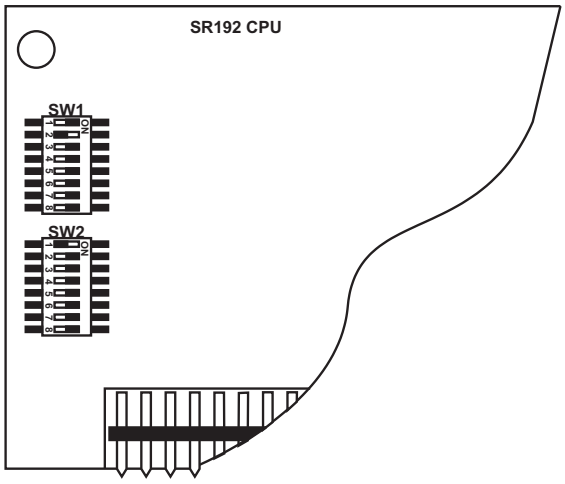

Figure 3-4 SR192A CPU Module Switch Settings

SW1							
8	7	6	5	4	3	2	1
LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0

Switch position definitions:

Position 1 through 8 corresponds to bits 0 through 7 of the logical address. The “ON” setting sets the corresponding bit of the logical address to a one (1).

A logical address setting of 255 (factory default), all positions set “ON”, sets the SR192A into dynamic addressing mode. A logical address setting between 1 and 254 sets the SR192A into static mode. A logical address of zero is reserved for the slot 0 controller and is invalid.

3.2.3.2 Interrupt Level, A32/A24 Switch Selection (SW2)

SW2							
8	7	6	5	4	3	2	1
Reserved				A24/A32	Interrupt Level		

Switch position definitions:

The binary encoded value of the first three switch positions of SW2 are used to assign the VXI interrupt level.

Position 3	Position 2	Position 1	VXI Interrupt Level
OFF	OFF	OFF	Disabled (none)
OFF	OFF	ON	Level One Selected (factory default)
OFF	ON	OFF	Level Two Selected
OFF	ON	ON	Level Three Selected
ON	OFF	OFF	Level Four Selected
ON	OFF	ON	Level Five Selected
ON	ON	OFF	Level Six Selected
ON	ON	ON	Level Seven Selected

Switch position 4 is used to select A32/A24 register mapping.

Position 4	Register Mapping
OFF	A32 Register Mapping (factory default)
ON	A24 Register Mapping

Positions 5 through 8 are factory reserved and should be set to off.

Figure 3-4 shows a interrupt level setting of one (factory default). A setting of zero disables the VXI interrupt generation.

3.3 VXI Test Points and Fuses

Figure 3-5 below is a locator diagram for test points and fuses located on the SR192A VXI module, part number 10532.

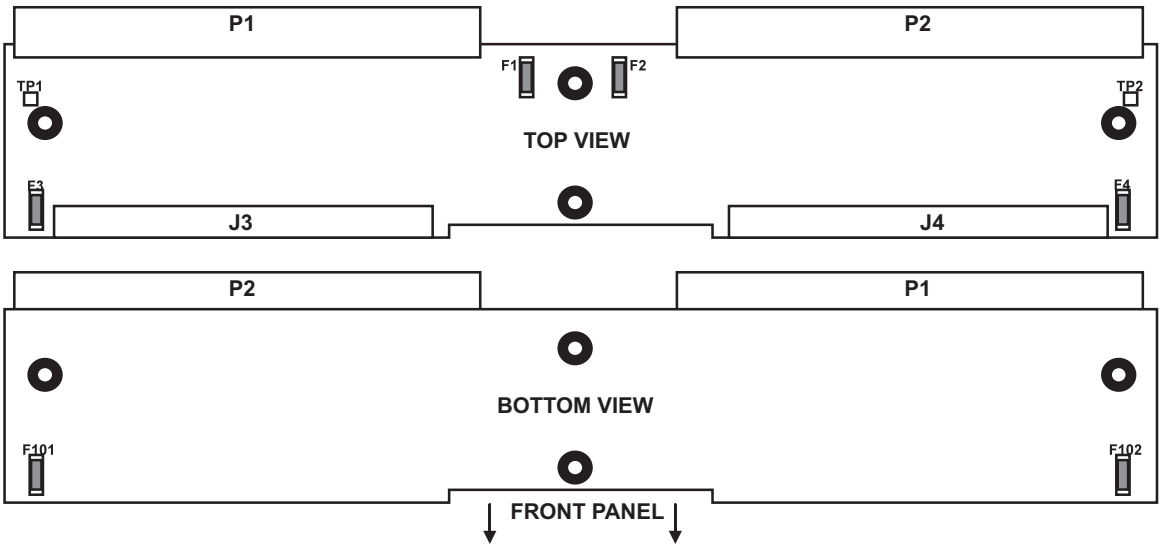

Figure 3-5 SR192A VXI Module Test Points and Fuses

3.3.1 VXI Test Point Description

Table 3-4 below describes the test points on the SR192A VXI module.

Mnemonic	Description
TP1	Signal ground
TP2	Signal ground

Table 3-4 SR192A VXI Module Test Points

3.3.2 VXI Fuse Description

Table 3-5 below describes the fuses on the VXI module for VXI backplane voltages used by the SR192A.

Fuse	Signal, Amps
F1	+5V, 10A
F2	+5V, 10A
F3	+12V, 2A
F4	+24V, 2A
F101	-24V, 2A
F102	-12V, 2A

Table 3-5 SR192A VXI Module Fuse Description

3.4 TSIO Jumper Description

The following sections describes the jumper selections for both types of SR192A TSIO modules, TTL (part number 20690) and differential/TTL (part number 20640).

3.4.1 TSIO Variable Voltage Jumper Description

Figure 3-6 shows the factory default jumper settings for TTL TSIO assembly.

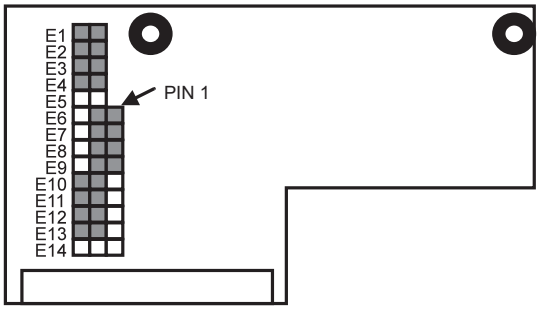

Figure 3-6 TSIO TTL (default) Jumper Locations

3.4.1.1 TSINPUTA1 Receiver Source (E1, E10)

The receiver for the TSINPUTA1 handshake signal is selected using jumpers E1 and E10. The TTL receiver is selected by installing a jumper in E1 and E10 pin 2 to pin 3 (factory default).

3.4.1.2 TSINPUTA2 Receiver Source (E2, E11)

The receiver for the TSINPUTA2 handshake signal is selected using jumpers E2 and E11. The TTL receiver is selected by installing a jumper in E2 and E11 pin 2 to pin 3 (factory default).

3.4.1.3 EXCLK1 Receiver Source (E3, E12)

The receiver for the EXCLK1 external clock signal is selected using jumpers E3 and E12. The TTL receiver is selected by installing a jumper in E3 and E12 pin 2 to pin 3 (factory default).

3.4.1.4 FCNTL1 Receiver Source (E4, E13, E14)

The receiver for the FCNTL1 control signal is selected using jumpers E4, E13 and E14. The TTL receiver is selected by installing a jumper in E4 and E13 pin 2 to pin 3 (factory default).

3.4.1.5 TSOUTA1 Driver Source (E7)

The driver for the TSOUTA1 signal is selected by using the E7 jumper. E7 pin 1 to pin 2 selects the TTL driver (factory default).

3.4.1.6 CLOCKA Driver Source (E8)

The driver for the CLOCKA signal is selected by using the E8 jumper. E8 pin 1 to pin 2 selects the TTL driver (factory default).

3.4.1.7 TSOUTA2 Driver Source (E9)

The driver for the TSOUTA2 signal is selected by using the E9 jumper. E9 pin 1 to pin 2 selects the TTL driver (factory default).

3.4.2 TSIO Differential/TTL Jumper Description

Figure 3-7 shows the factory default jumper settings for the differential/TTL TSIO assemble.

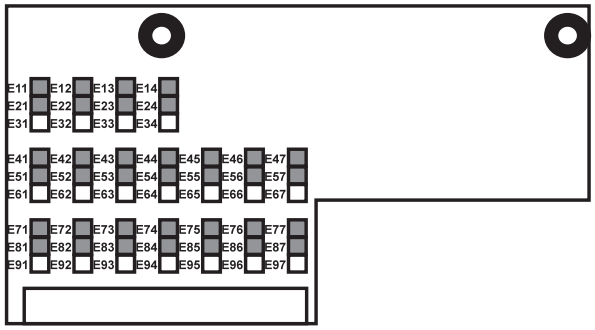

Figure 3-7 TSIO Differential/TTL (default)Jumper Locations

3.4.2.1 TSINPUTA1 Receiver Source (E14,E24,E34,E44,E54,E64,E74,E84,E94)

The receiver for the TSINPUTA1 handshake signal is selected using jumpers E14 through E94. The TTL receiver is selected by installing jumpers between E14 and E24, E44 and E54, E74 and E84 (factory default). The differential receiver is selected by installing jumpers between E24 and E34, E54 and E64, E84 and E94.

3.4.2.2 TSINPUTA2 Receiver Source (E13,E23,E33,E43,E53,E63,E73,E83,E93)

The receiver for the TSINPUTA2 handshake signal is selected using jumpers E13 through E93. The TTL receiver is selected by installing jumpers between E13 and E23, E43 and E53, E73 and E83 (factory default). The differential receiver is selected by installing jumpers between E23 and E33, E53 and E63, E83 and E93.

3.4.2.3 EXCLK1 Receiver Source (E12,E22,E32,E42,E52,E62,E72,E82,E92)

The receiver for the EXCLK1 external clock signal is selected using jumpers E12 through E92. The TTL receiver is selected by installing a jumper between E12 and E22, E42 and E52, E72 and E82 (factory default). The differential receiver is selected by installing jumpers between E22 and E32, E52 and E62, E82 and E92.

3.4.2.4 FCNTL1 Receiver Source (E11,E21,E31,E41,E51,E61,E71,E81,E91)

The receiver for the FCNTL1 control signal is selected using jumpers E11 through E91. The TTL receiver is selected by installing a jumper between E11 and E21, E41 and E51, E71 and E81 (factory default). The differential receiver is selected by installing jumpers between E21 and E31, E51 and E61, E81 and E91.

3.4.2.5 TSOUTA1 Driver Source (E46,E56,E66,E76,E86,E96)

The driver for the TSOUTA1 signal is selected by using E46 through E96 jumpers. Jumpers between E46 and E56, E76 and E86 selects the TTL driver (factory default). Jumpers between E56 and E66, E86 and E96 selects the differential driver.

3.4.2.6 CLOCKA Driver Source (E47,E57,E67,E77,E87,E97)

The driver for the CLOCKA signal is selected by using E47 through E97 jumpers. Jumpers between E47 and E57, E77 and E87 selects the TTL driver (factory default). Jumpers between E57 and E67, E87 and E97 selects the differential driver.

3.4.2.7 TSOUTA2 Driver Source (E45,E55,E65,E75,E85,E95)

The driver for the TSOUTA2 signal is selected by using E45 through E95 jumpers. Jumpers between E45 and E55, E75 and E85 selects the TTL driver (factory default). Jumpers between E55 and E65, E85 and E95 selects the differential driver.

3.5 Module Installation

Along with the CPU, VXI and TSIO modules, each SR192A baseboard can optionally house up to two timing modules, twelve I/O modules and one MFC Accessory module.

Figure 3-8 below illustrates the slot positions of the SR192A and their reference designators.

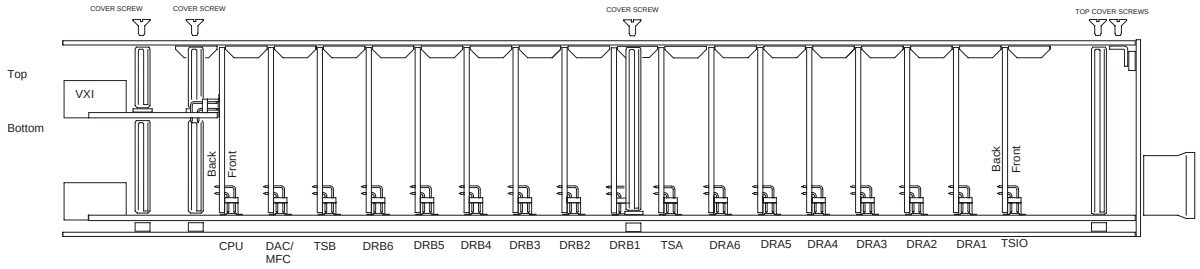

Figure 3-8 SR192A Slot Position Side View

Perform the following steps to add or replace an SR192A module:

Step 1. Using ESD protocols remove the SR192A from the VXI chassis.

Step 2. Remove the top cover black anodized screws, refer to Figure 3-8.

Step 3. If replacing either the CPU or VXI module, remove the spacers that hold the VXI module.

Step 4. Remove the module by grasping at each corner and gently rocking forward and back while pulling it away from the baseboard.

Step 5. Insert the module in the desired slot by lining up the connectors and gently pushing down. All SR192A modules except the VXI and TSIO are keyed along the associated mating connector. If the module cannot be inserted, check for bent pins and make certain the pins are aligned with the mating connector on the baseboard.

WARNING

Make sure the connectors are aligned and in the proper slot position. It is possible to mis-align or force even a keyed module into the wrong slot or pin number.

Step 6. Reinstall spacers and washers if applicable.

Step 7. Reinstall top cover.

3.6 Termination Options

Table 3-6 below list the termination value and location of each resistor for the front panel signals.

Connector	Signal	Logic	Termination	Location
J1-J6	CH1-CH192	I/O Module Specific		I/O Module
J1-J6	SIGMON	LVTTL	NONE	I/O Module
J7	System master/slave connector, see section 3.1.4			
J8	**TSIO Assembly 20690 Signals**			
	TSOUTA1	TTL	Series 47Ω	TSIO, R23
	TSOUTA2	TTL	Series 47Ω	TSIO, R22
	CLOCKA	TTL	Series 47Ω	TSIO, R24
	TSINPUTA1	TTL	Parallel to GND	TSIO, Not Installed, R2
	TSINPUTA2	TTL	Parallel to GND	TSIO, Not Installed, R5
	EXCLK1	TTL	Parallel to GND	TSIO, Not Installed, R1
	FCNTL1	TTL	Parallel to GND	TSIO, Not Installed R4
	TSIO Assembly 20640Signals			
	TSOUTA1	TTL	Series 47Ω	TSIO, R5
		Differential	None	NA
	TSOUTA2	TTL	Series 47Ω	TSIO, R3
		Differential	None	NA
	CLOCKA	TTL	Series 47Ω	TSIO, R7
		Differential	None	NA
	TSINPUTA1	TTL	10KΩ to GND	TSIO, R6
		Differential	120Ω parallel	TSIO, R11
	TSINPUTA2	TTL	10KΩ to GND	TSIO, R4
		Differential	120Ω parallel	TSIO, R10
	EXCLK1	TTL	10KΩ to GND	TSIO, R2
		Differential	120Ω parallel	TSIO, R9
	FCNTL1	TTL	10KΩ to GND	TSIO, R1
		Differential	120Ω parallel	TSIO, R8
	Baseboard Signals			
	TSOUTA3-5 TSOUTB1-5	TTL	Series 47Ω	MB, U2
	TSINPUTB1	TTL	10KΩ to GND	MB, R42
	TSINPUTB2	TTL	10KΩ to GND	MB, R41
	EXCLK2	TTL	NONE	MB, R83
	TSABUSY	TTL	NONE	NA
	TSBBUSY	TTL	NONE	NA
	SYNCA	LVTTL	NONE	NA
	SYNCB	LVTTL	NONE	NA
	FCNTL2	TTL	10KΩ to GND	MB, R65
	CLOCKB	TTL	Series 47Ω	MB, R67
	PRBDAT	TTL	NONE	NA
	UUTRST	TTL	Series 47Ω	MB, R79
	CLKRSTE	TTL	NONE	NA
SMA	CLKOUTA	LVTTL	Series 47Ω	TSA, R216
	CLKOUTB	LVTTL	Series 47Ω	TSB, R216
	PGMCLK1	TTL	Series 47Ω	MFC, U5
	PGMCLK2	TTL	Series 47Ω	MFC, U5
	PGMCLK2V	Variable Voltage	Series 47Ω	MFC, U5
	CLKREF	TTL	82Ω to GND	MFC, R113

Table 3-6 Front Panel Signal Termination Location and Values

4 Functional Description

The SR192A System is a “C” size, dual slot, VXI module. It was designed to be a modular system housing digital I/O modules, timing control modules and the VXI system circuitry. The Baseboard System is comprised of the front panel, baseboard and the CPU/VXI modules. The I/O modules plug into connectors located on the baseboard and are field replaceable.

Figure 4-1 depicts the major logic elements of the SR192A system.

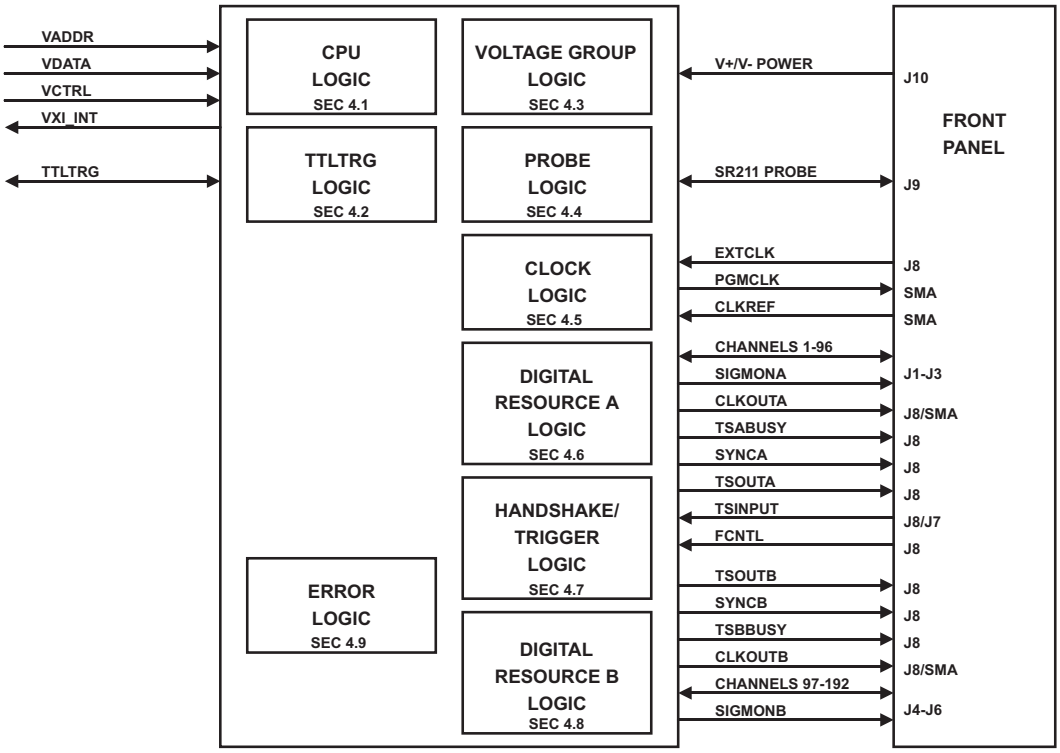

Figure 4-1 SR192A Block Diagram

The following list describes the functional blocks shown in figure above.

1. CPU logic — This logic controls the VXI backplane interface as well as the local CPU interface which is used to program the SR192A and its components.
2. TTLTRG logic — This logic allows the user to enable/disable SR192A signals to/from the VXI TTLTRG bus.
3. Voltage group/DAC logic — This logic distributes the external power inputs and internal reference levels to the Digital Resource and TSIO LOGIC.
4. Probe logic — This logic routes the SR211 probe signals to the FRONT PANEL.
5. Clock logic — This logic generates clock signals for the digital resources and also interfaces to the front panel.
6. Digital Resource A logic — This logic which consists of the TSA timing module and DRA1 through DRA6 I/O modules provides the stimulus/response logic for channels 1 through 96.
7. Handshake/trigger logic — This logic is used to distribute and synchronize the handshake signals to both Digital Resource blocks.
8. Digital Resource B logic — This logic which consists of the TSB timing module and DRB1 through DRB6 I/O modules provides the stimulus/response logic for channels 97 through 192.
9. Error logic — This logic monitors the real time error bits from Digital Resource A and records response error data.

The following list describes the signals shown in figure 4-1.

1. VADDR — The address bus from the VXI bus backplane.
2. VDATA — The data bus from the VXI bus backplane.
3. VCTRL — The control bus from the VXI bus backplane.
4. VXI_INT — Selected VXI interrupt signal from SW1.
5. TTLTRG — The TTL Trigger bus from the VXI bus backplane.

6.	V+/V- POWER	The positive and negative input voltage used to supply power to the variable voltage driver/receiver modules.
7.	SR211 PROBE	The signals used to control the SR211 probe pod.
8.	EXTCLK	Two external clocks routed to both timing modules.
9.	PGMCLK	The three programmable clock outputs (PGMCLK1, PGMCLK2 and PGMCLK2V).
10.	CLKREF	External clock reference input (CLKREF) for the PGMCLKs.
11.	CHANNELS 1-96	96 I/O signals routed to DRA1 through DRA6 I/O module slots.
12.	SIGMONA	6 output signals. One signal routed to each I/O module DRA slot.
13.	CLKOUTA	Selected clock for digital resource A.
14.	TSABUSY	Active low signal that indicates that digital resource A is running.
15.	SYNCA	Programmable output trigger from the TSA timing module.
16.	TSOUTA	General purpose output handshake/trigger signals from the TSA timing module.
17	TSINPUT	Five general purpose trigger/handshake inputs, two routed to TSA and two routed to TSB. The fifth routed to both for synchronous triggering in linked and master/slave mode.
18.	FCNTL	Two external I/O control signals routed to all I/O modules and error logic.
19.	TSOUTB	General purpose output handshake/trigger signals from the TSB timing module.
20.	SYNCB	Programmable output trigger from the TSB timing module.
21.	TSBBUSY	Active low signal that indicates that digital resource B is running.
22.	CLKOUTB	Selected clock for digital resource B.
23.	CHANNELS 97-192	96 I/O signals routed to DRB1 through DRB6 I/O module slots.
24.	SIGMONB	6 output signals. One signal routed to each I/O module DRB slot.

The following sections describe the nine logic elements of the SR192A.

4.1 CPU Logic

The CPU logic performs the VXI interface management as well as the SCPI command language control.

The VXI interface management involves the A16 registers and the Word Serial (WS) commands that the SR192A supports. The SR192A Operators manual describes the WS commands that the SR192A responds to.

The SCPI command language control includes the command parser as well as the execution control software. The SR192A Operators manual lists all the SCPI commands of the SR192A.

Figure 4-2 shows the CPU logic block diagram.

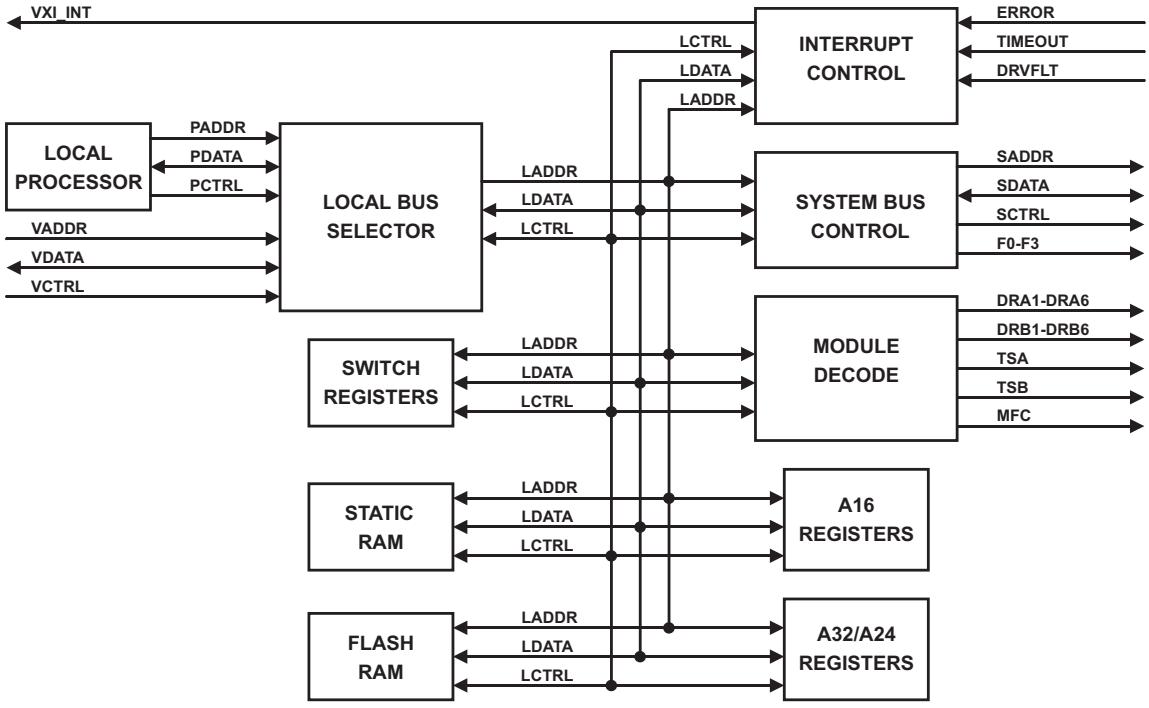

Figure 4-2 CPU Logic Block Diagram

The following list describes the functional blocks above.

1.	Local processor	The local processor manages the VXI interface as well as SCPI command parser.
2.	Local bus selector	This logic controls the local bus arbitration between the VXI bus and the processor bus.

3. Switch registers — The switch register are read by the CPU on power-up in order to assign the logical address and VXI interrupt level.
4. Static RAM — The static RAM is used by the SCPI parser and execution firmware as allocable heap memory. The static RAM is also used to update the flash firmware.
5. Flash RAM — The flash RAM contains the local processor code and SCPI parser.
6. Interrupt control — VXI interrupts can be generated by real time events or by the local processor.
7. System bus control — This logic manages byte/word data sent to or read from any of the I/O of timing modules.
8. Module decode — The module decodes along with the function code (F0-F3) identifies a specific module and register page.
9. A16 registers — The A16 registers are defined by the VXI standard, see appendix B.
10. A32/A24 registers — The A32/A24 registers are defined in appendix B.

The following list describes the signals from figure 4-2.

1. VXI_INT — Selected VXI interrupt line.
2. PADDR — Processor address bus.
3. PDATA — Processor data bus.
4. PCTRL — Processor control bus.
5. VADDR — VXI address bus.
6. VDATA — VXI data bus.
7. VCTRL — VXI control bus.
8. LADDR — Local address bus.
9. LDATA — Local data bus.
10. LCTRL — Local control bus.
11. ERROR — Real time error from the Digital Resources.
12. TIMEOUT — Input trigger timeout from the Digital Resources.
13. DRVFLT — Variable Voltage drivers over current flag.
14. SADDR — Selected address bus to the timing modules.
15. SDATA — Selected data bus to the timing and I/O modules.
16. SCTRL — Selected control bus to the timing and I/O modules.
17. F0-F3 — Function code select signals.
18. DRA1-DRA6 — Digital Resource A I/O module decodes.
19. DRB1-DRB6 — Digital Resource B I/O module decodes.
20. TSA — 7Digital Resource A timing module decode.
21. TSB — Digital Resource B timing module decode.
22. MFC — Reference/multifunction module decode.

4.2 TTLTRG Logic

The TTLTRG bus from the VXI backplane is an open collector, daisy chained bus used for cross-triggering multiple instruments.

Figure 4-3 shows the TTLTRG logic block diagram.

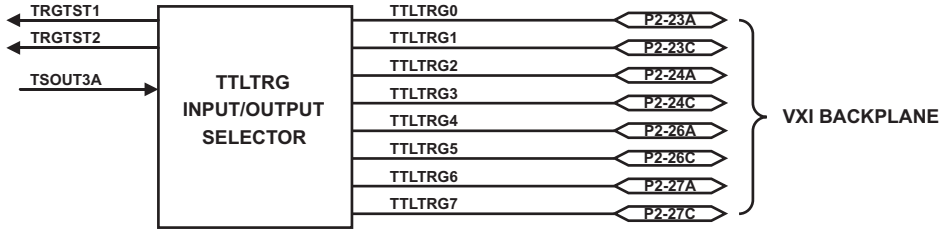

Figure 4-3 TTLTRG Logic Block Diagram

The following list describes the functional blocks shown in the figure above.

1. TTLTRG input/output select — This logic selects routs signals to and from the VXI TTLTRG bus.

The following list describes the signals listed in figure 4-3.

1. TRGTST1 — Input trigger sourced by one of the VXI TTLTRG lines that is routed to the timing module of digital resource A (TSA). Refer to section 4.7.2.
2. TRGTST2 — Input trigger sourced by one of the VXI TTLTRG lines that is routed to the timing module of digital resource B (TSB). Refer to section 4.7.2.
3. TSOUT3A — One of the five output triggers from the TSA timing module.
4. TTLTRG0-TTLTRG7 — Eight TTL trigger lines to/from the VXI backplane.

4.3 Voltage Group Logic

Several of Talon's SR192A I/O modules contain Variable Voltage drivers/receivers. These Variable Voltage driver/receivers require external voltage to power the ICs.

Figure 4-4 shows the voltage group logic of the SR192A baseboard.

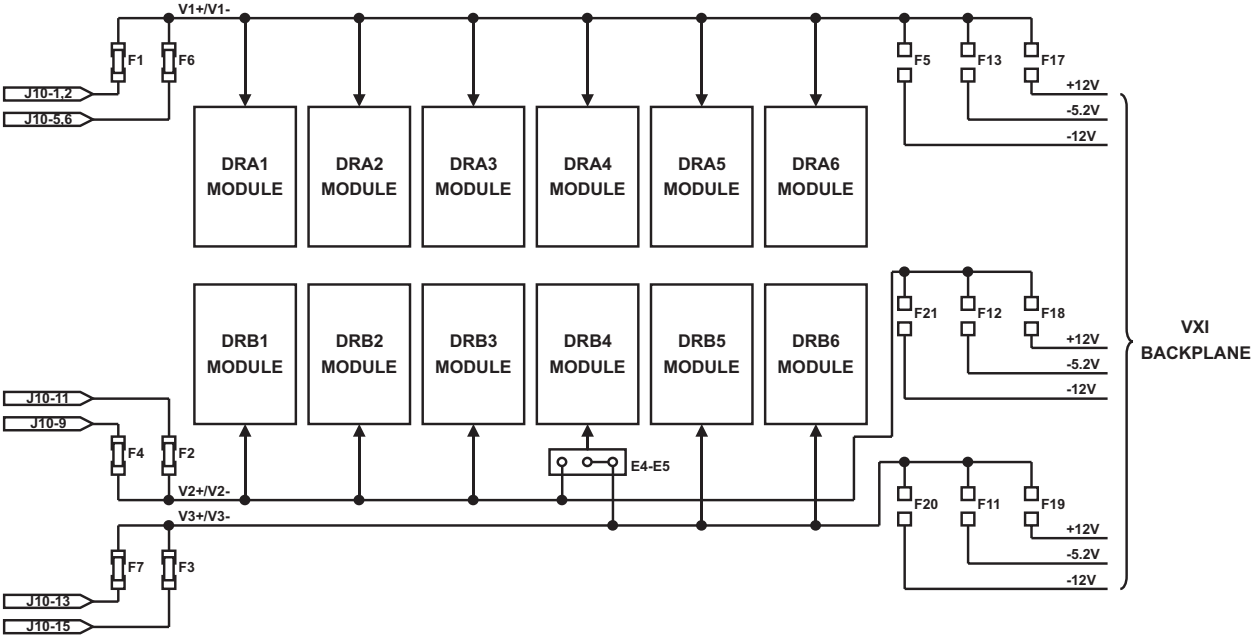

Figure 4-4 Voltage Group Logic Block Diagram

The following list describes the functional blocks shown in the figure above.

1.	DRA1 module	The logic and memories for I/O channels 1-16.
2.	DRA2 module	The logic and memories for I/O channels 17-32.
3.	DRA3 module	The logic and memories for I/O channels 33-48.
4.	DRA4 module	The logic and memories for I/O channels 49-64.
5.	DRA5 module	The logic and memories for I/O channels 65-80.
6.	DRA6 module	The logic and memories for I/O channels 81-96.
7.	DRB1 module	The logic and memories for I/O channels 97-112.
8.	DRB2 module	The logic and memories for I/O channels 113-128.
9.	DRB3 module	The logic and memories for I/O channels 129-144.
10.	DRB4 module	The logic and memories for I/O channels 145-160.
11.	DRB5 module	The logic and memories for I/O channels 161-176.
12.	DRB6 module	The logic and memories for I/O channels 177-192.

The following list describes the signals shown in figure 4-4.

1.	F<n>	Baseboard fuses used for selecting the voltage source of the variable voltage modules.
2.	V1+/V1-	Voltage group one positive and negative input voltages.
3.	+12V	+12 volt signal from the VXI backplane.
4.	-5.2V	-5.2 volt signal from the VXI backplane.
5.	-12V	-12 volt signal from the VXI backplane.
6.	E4-E5	Jumpers used to select the voltage group source for DRB4.
7.	V2+/V2-	Voltage group two positive and negative input voltages.
8.	V3+/V3-	Voltage group three positive and negative input voltages.

4.4 Probe Logic

Talons SR210 MFC Accessory module contains interface logic for the SR211 Probe Pod.

Figure 4-6 shows the probe logic of the SR192A baseboard.

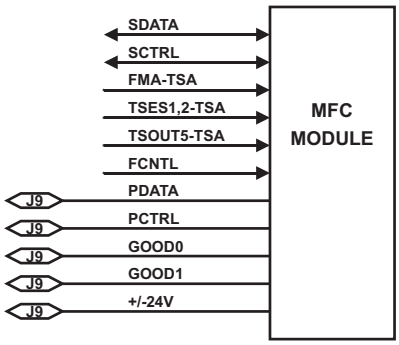

Figure 4-6 Probe Logic Block Diagram

The following list describes the functional blocks listed above.

1. MFC — The logic and drivers for SR211 probe pod interface.

The following list describes the signals shown in figure 4-6.

1. J9 — Front panel connector I/O.
5. SDATA — Selected data bus to the timing and I/O modules.
6. SCTRL — Selected control bus to the timing and I/O modules.
7. FMA-TSA — Memory address bus from the TSA timing module.
8. TSES1,2-TSA — Two input strobe signals from the TSA timing module that can be selected as the probe data clock.
9. TSOUT5-TSA — General purpose output signal from the TSA timing module that can be selected as the probe data clock.
10. FCNTL — Two external I/O control signals. routed to all I/O modules that can be selected as the probe data strobe.
11. PDATA — Probe data bus used to send/receive commands or data to the SR211 pod.
12. PCTRL — Probe control bus used to send/receive commands or data to the SR211 pod.
13. GOOD0 — Input signal from the SR211 pod that indicates a valid low signal.
14. GOOD1 — Input signal from the SR211 pod that indicates a valid high signal.
15. +/-24V — Fused +24V and -24V from the VXI backplane.

4.5 Clock Logic

The timing modules on the SR192A operate using a single clock to which the stimulus/response addresses and control signals are synchronized. This clock, called TS_CLK, can be selected from several sources.

Figure 4-5 shows the clock logic of the SR192A baseboard.

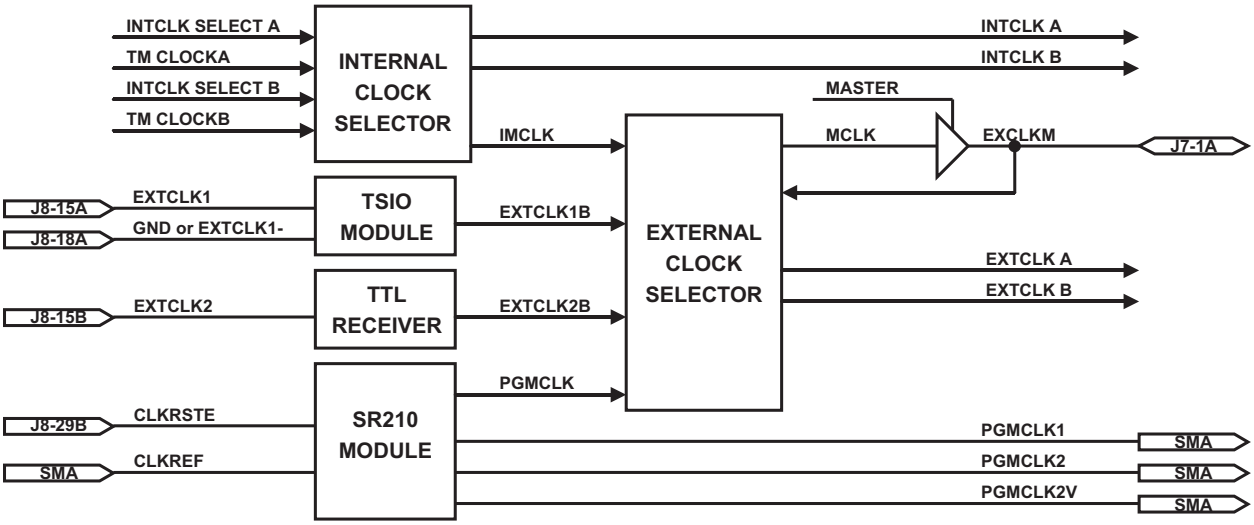

Figure 4-5 Clock Logic Block Diagram

The following list describes the functional blocks shown in the figure above.

1. INTERNAL CLK SELECTOR — This logic generates the internal 10, 20 or 50 MHz clock frequency for both TSA and TSB timing modules.
2. TSIO MODULE — Receiver for EXTCLK1 for the timing modules.
3. TTL RECEIVER — Receiver for EXTCLK2 for the timing modules.
4. SR210 MODULE — SR210 accessory module.

5. EXTERNAL CLK SELECTOR — This logic selects the external clock source for both TSA and TSB timing modules.

The following list describes the signals shown in the figure 4-5.

1. INTCLK SELECT A — Signal from TSA that selects INTCLK A source.
2. TM CLOCKA — Timing Module A internal clock.
3. TM CLOCKB — Timing Module B internal clock.
4. INTCLK SELECT B — Signal from TSB that selects INTCLK B source.
5. EXTCLK1 — TTL, Variable Voltage or differential clock one from the front panel.
6. GND or EXTCLK1- — Differential compliment of EXCLK1 or signal ground for TTL and Variable Voltage.
7. EXTCLK2 — TTL clock two from the front panel.
8. CLKRSTE — TTL clock reset signal for the programmable clock logic.
9. CLKREF — TTL clock generator reference signal for the programmable clock logic.
10. 100 MHz — Internal clock used to generate the 50/20/10 MHz clocks to the timing modules.
11. IMCLK — Internal J7 master bus clock (EXCLKM) source.
12. EXTCLK1B — Buffered external clock one signal.
13. EXTCLK2B — Buffered external clock two signal.
14. PGMCLK — Programmable clock signal from the SR210 installed in the MFC slot.
15. MASTER — Signal used to enable the driver for the synchronized clock routed to the J7 connector.
16. MCLK — Selected master clock signal. Valid choices are EXTCLK1, EXTCLK2, IMCLK or PGMCLK.
17. INTCLK A — Selected TSA internal clock signal.
18. INTCLK B — Selected TSB internal clock signal.
19. EXTCLKM — Synchronized clock for master/slave functions.
20. EXTCLK A — Selected TSA external clock signal. Valid choices are EXTCLK1, EXTCLK2, EXTCLKM or PGMCLK.
21. EXTCLK B — Selected TSB external clock signal. Valid choices are EXTCLK1, EXTCLK2, EXTCLKM or PGMCLK.
22. PGMCLK1 — TTL PGMCLK1 output.
23. PGMCLK2 — TTL PGMCLK2 output.
24. PGMCLK2V — Variable Voltage +8V to -8V PGMCLK2 output.

4.6 Digital Resource A Logic

The SR192A can contain two independent Digital Resources which are comprised of a timing module and one or more I/O modules. Digital Resource A can be synchronized to an external source through the J7 master/slave connector.

Figure 4-7 shows the Digital Resource A logic of the SR192A.

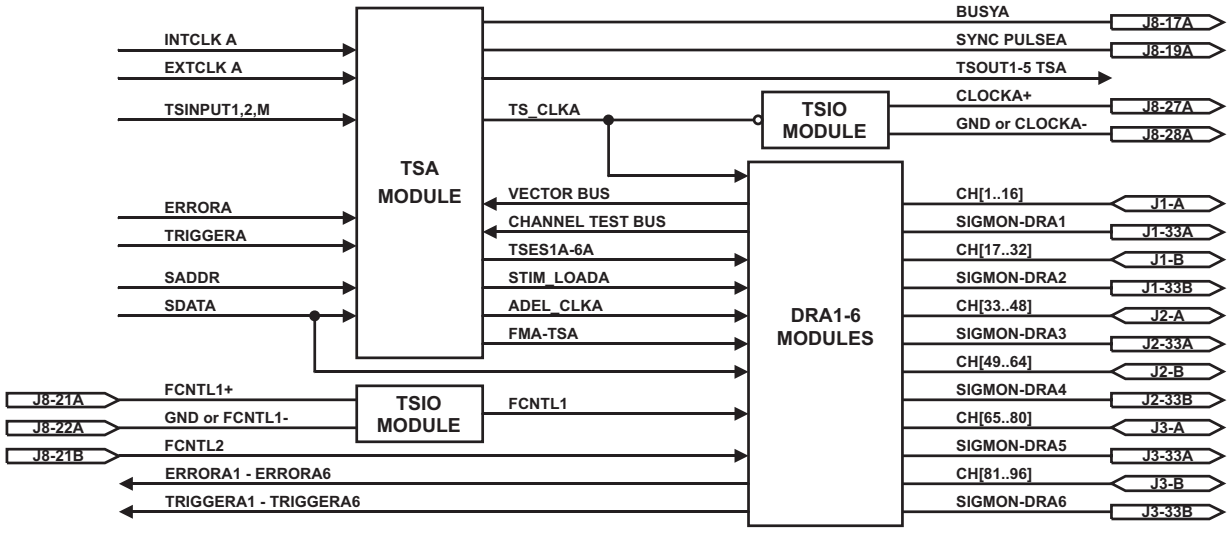

Figure 4-7 Digital Resource A Logic Block Diagram

The following list describes the functional blocks shown in the figure above.

1. TSA MODULE — Timing module that generates the word address and control signals for I/O channels 1 through 96.

2.	TSIO MODULE	Driver/Receiver module for the timing module I/O.
3.	DRA1-6 MODULE	The logic and memories for I/O channels 1-96.

The following list describes the signals shown in figure 4-7

1.	INTCLK A	Selected internal clock.
2.	EXTCLK A	Selected external or J7 master bus clock.
3.	TSINPUT1A,2A,M	Test input one for TSA.
4.	ERRORA	Error flag from the error logic, see section 4.9
5.	TRIGGERA	Trigger flag from the trigger logic, see section 4.9.
6.	SADDR	Selected address bus to the timing modules.
7.	SDATA	Selected data bus to the timing and I/O modules.
8.	FCNTL1+	TTL, Variable Voltage or differential strobe/enable one to the I/O modules. Differential input inverted.
9.	GND or FCNTL1-	Differential compliment of FCNTL1 or signal ground for TTL and Variable Voltage.
10.	FCNTL2	TTL I/O strobe/enable two to the I/O modules.
11.	ERRORA1 - ERRORA6	Real time error flag from each I/O module.
12.	TRIGGERA1 - TRIGGERA6	Real time compare flag from each I/O module.
13.	TS_CLKA	Selected TSA timing clock.
14.	VECTOR BUS	The vector bus allows the user to select four of the receiver channels and route them to the timing module as a vector index for the sequence jump logic.
15.	CHANNEL TEST BUS	The channel test bus allows the user to select two of the receiver channels and route them to the timing module as handshake signals.
16.	TSES1-6A	Six internal stimulus/response control signals.
17.	STIM_LOADA	I/O module control signal used to load stimulus memory and latch the response address.
18.	ADEL_CLKA	I/O module control signal used to latch the response address.
19.	FMA-TSA	I/O module stimulus/response memory address bus.
20.	FCNTL1	External stimulus/response control signal.
21.	TSABUSY	TSA running signal.
22.	SYNC PULSEA	Programmable output sync.
23.	TSOUT1-5 TSA	Output handshake/trigger signals, see section 4.7.1.
24.	CLOCKA+	TTL, Variable Voltage or differential output of TS_CLKA.
25.	GND or CLOCKA-	Differential compliment of TS_CLKA or signal ground for TTL and Variable Voltage.
26.	CH[1..16]	I/O channels 1-16.
27.	SIGMON-DRA1	Signal monitor for DRA1.
28.	CH[17..32]	I/O channels 17-32.
29.	SIGMON-DRA2	Signal monitor for DRA2.
30.	CH[33..48]	I/O channels 33-48.
31.	SIGMON-DRA3	Signal monitor for DRA3.
32.	CH[49..64]	I/O channels 49-64.
33.	SIGMON-DRA4	Signal monitor for DRA4.
34.	CH[65..80]	I/O channels 65-80.
35.	SIGMON-DRA5	Signal monitor for DRA5.
36.	CH[81..96]	I/O channels 81-96.
37.	SIGMON-DRA6	Signal monitor for DRA6.

4.7 Handshake/Trigger Logic

The SR192A routes output and input handshake/trigger signals to the two timing modules, TSA and TSB. Each timing module has five general purpose output signals (TSOUT1 through TSOUT5) and two test input signals (TSINPUT1 and TSINPUT2). The following sections describes the baseboard routing logic for these signals.

4.7.1 Output Handshake/Trigger Logic (TSOUT)

Figure 4-8 shows the output logic of the SR192A baseboard.

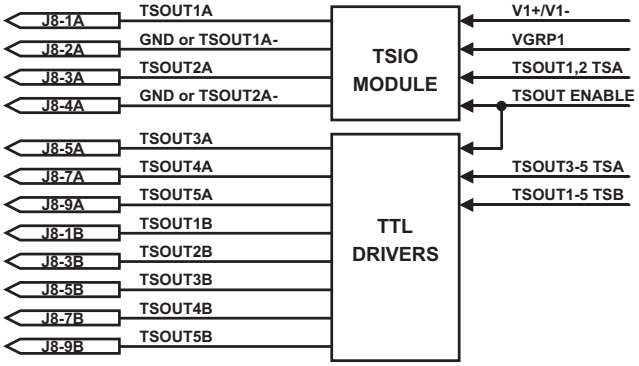

Figure 4-8 Output Trigger Block Diagram

The following list describes the functional blocks shown in the figure above.

1.	TSIO module	Drivers for TSOUT1 and TSOUT2 from the TSA timing module.
2.	TTL drivers	Drivers for TSOUT3 through TSOUT5 from TSA and TSOUT1 through TSOUT5 from TSB.

The following list describes the signals shown in figure 4-8.

1.	TSOUT1A+	TTL, Variable Voltage or differential output of TSOUT1 TSA.
2.	GND or TSOUT1A-	Differential compliment of TSOUT1 TSA or signal ground for TTL and Variable Voltage.
3.	TSOUT2A+	TTL, Variable Voltage or differential output of TSOUT2 TSA.
4.	GND or TSOUT2A-	Differential compliment of TSOUT2 TSA or signal ground for TTL and Variable Voltage.
5.	TSOUT3A	TTL output of TSOUT3 TSA.
6.	TSOUT4A	TTL output of TSOUT4 TSA.
7.	TSOUT5A	TTL output of TSOUT5 TSA.
8.	TSOUT1B	TTL output of TSOUT1 TSB.
9.	TSOUT2B	TTL output of TSOUT2 TSB.
10.	TSOUT3B	TTL output of TSOUT3 TSB.
11.	TSOUT4B	TTL output of TSOUT4 TSB.
12.	SOUT5B	TTL output of TSOUT5 TSB.
13.	V1+/V1-	Voltage group one input supply for TSOUT1A and TSOUT2A Variable Voltage outputs.
14.	VGRP1	Voltage group one reference signals for TSOUT1A and TSOUT2A Variable Voltage outputs.
15.	TSOUT1-TSA	TSOUT1 signal from the TSA timing module.
16.	TSOUT2-TSA	TSOUT2 signal from the TSA timing module.
17.	TSOUT ENABLE	User controlled output enable signal.
18.	TSOUT3-TSA	TSOUT3 signal from the TSA timing module.
19.	TSOUT4-TSA	TSOUT4 signal from the TSA timing module.
20.	TSOUT5-TSA	TSOUT5 signal from the TSA timing module.
21.	TSOUT1-TSB	TSOUT1 signal from the TSB timing module.
22.	TSOUT2-TSB	TSOUT2 signal from the TSB timing module.
23.	TSOUT3-TSB	TSOUT3 signal from the TSB timing module.
24.	TSOUT4-TSB	TSOUT4 signal from the TSB timing module.
25.	TSOUT5-TSB	TSOUT5 signal from the TSB timing module.

4.7.2 Test Input Handshake/Trigger Logic (TSINPUT)

Figure 4-9 shows the test input logic of the SR192A baseboard.

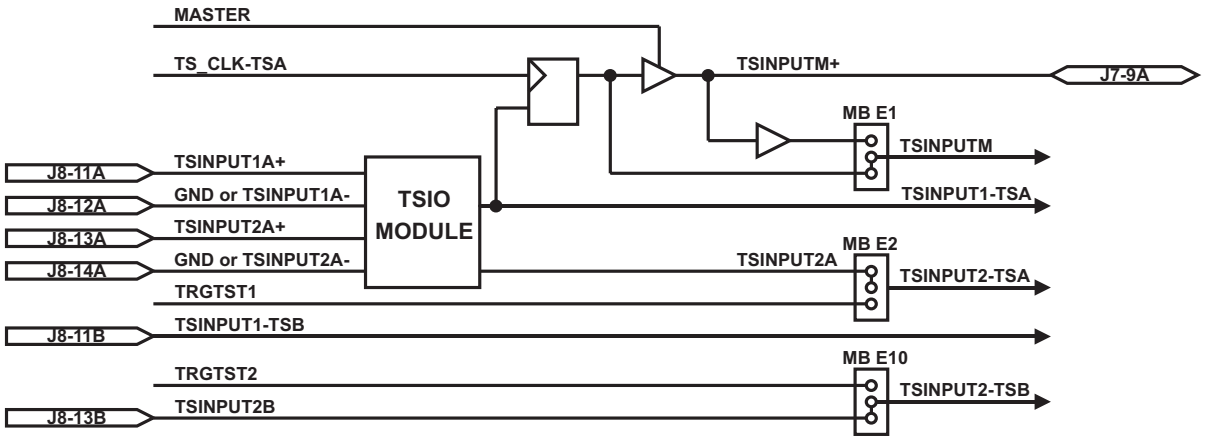

Figure 4-9 Input Trigger Logic Block Diagram

The following list describes the functional blocks shown in the figure above.

1.	TSIO module	Receivers for TSINPUT1A and TSINPUT2A for the TSA timing module.
3.	MB E1	Baseboard jumper block E1, see section 3.1.2.2.
4.	MB E2	Baseboard jumper block E2, see section 3.1.2.3.
5.	MB E10	Baseboard jumper block E10, see section 3.1.2.5.

The following list describes the signals shown in the figure 4-9 above.

1.	MASTER	Signal used to enable the driver for the synchronized input trigger routed to the J7 connector.
2.	TS_CLK-TSA	Timing set clock from the TSA timing module used to synchronize theTSINPUT1A signal.
3.	TSINPUT1A+	TTL, Variable Voltage or differential test input one to the TSA timing module.
4.	GND or TSINPUT1A-	Differential compliment of TSINPUT1A or signal ground for TTL and Variable Voltage.
5.	TSINPUT2A+	TTL, Variable Voltage or differential test input two to the TSB timing module.
6.	GND or TSINPUT2A-	Differential compliment of TSINPUT2A or signal ground for TTL and Variable Voltage.
7.	TRGTST1	Selected TTL trigger from the VXI backplane, see section 4.2.
8.	TSINPUT1-TSB	TTL test input one to the TSB timing module.

9.	TRGTST2	Selected TTL trigger from the VXI backplane, see section 4.2.
10.	TSINPUT2B	TTL test input two to the TSB timing module.
11.	TSINPUTM+	Master/slave test signal from the front panel.
12.	TSINPUT2A	Test input two routed to the TSA timing module.
13.	TSINPUTM	Selected master/slave test signal to the timing modules.
14.	TSINPUT1-TSA	Test input one to the TSA timing module.
15.	TSINPUT2-TSA	Test input two to the TSA timing module.
16.	TSINPUT2-TSB	Selected test input two routed to the TSB timing module.

4.8 Digital Resource B Logic

Digital resource B can be synchronized to either digital resource A or an external source through the J7 master/slave connector.

Figure 4-10 shows the Digital Resource B logic of the SR192A.

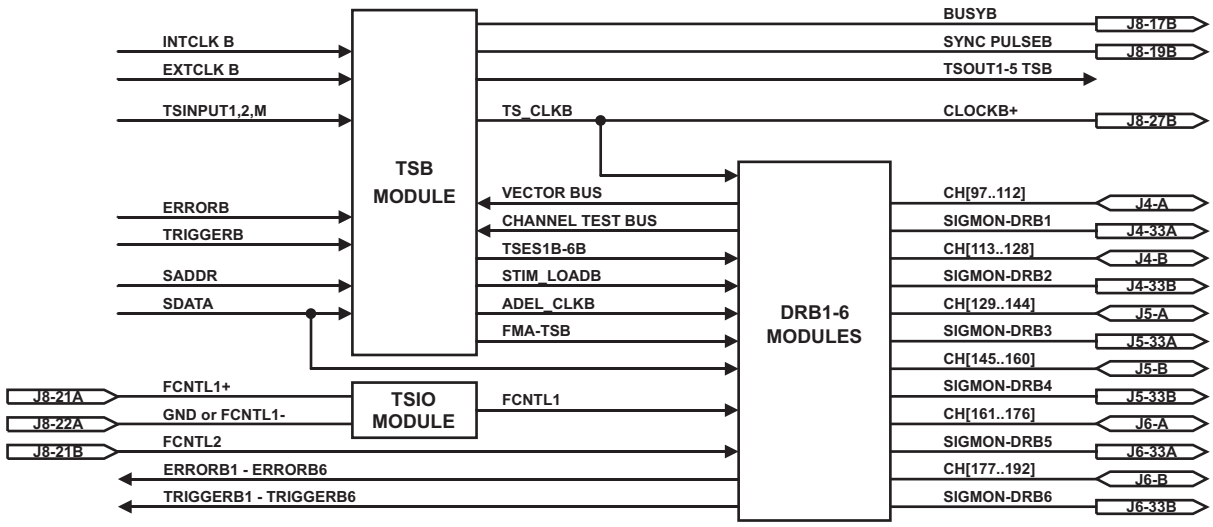

Figure 4-10 Digital Resource B Logic Block Diagram

The following list describes the functional blocks shown in the figure above.

1.	TSA MODULE	Timing module that generates the word address and control signals for I/O channels 1 through 96.
2.	TSIO MODULE	Driver/Receiver module for the timing module I/O.
3.	DRB1-6 MODULE	The logic and memories for I/O channels 97-192.

The following list describes the signals shown in figure 4-7

1.	INTCLK B	Selected internal clock.
2.	EXTCLK B	Selected external or J7 master bus clock.
3.	TSINPUT1B,2B,M	Test inputs for TSB.
4.	ERRORB	Error flag from the error logic, see section 4.9
5.	TRIGGERB	Trigger flag from the trigger logic, see section 4.9.
6.	SADDR	Selected address bus to the timing modules.
7.	SDATA	Selected data bus to the timing and I/O modules.
8.	FCNTL1+	TTL, Variable Voltage or differential strobe/enable one to the I/O modules. Differential input inverted.
9.	GND or FCNTL1-	Differential compliment of FCNTL1 or signal ground for TTL and Variable Voltage.
10.	FCNTL2	TTL I/O strobe/enable two to the I/O modules.
11.	ERROR1B - ERROR6B	Real time error flag from each I/O module.
12.	TRIGGER1B - TRIGGER6B	Real time compare flag from each I/O module.
13.	TS_CLKB	Selected TSB timing clock.
14.	VECTOR BUS	The vector bus allows the user to select four of the receiver channels and route them to the timing module as a vector index for the sequence jump logic.
15.	CHANNEL TEST BUS	The channel test bus allows the user to select two of the receiver channels and route them to the timing module as handshake signals.
16.	TSES1-6B	Six internal stimulus/response control signals.
17.	STIM_LOADB	I/O module control signal used to load stimulus memory and latch the response address.
18.	ADEL_CLKB	I/O module control signal used to latch the response address.
19.	FMA-TSB	I/O module stimulus/response memory address bus.
20.	FCNTL1	External stimulus/response control signal.
21.	TSBBUSY	TSA running signal.
22.	SYNC PULSEB	Programmable output sync.
23.	TSOUT1-5 TSB	Output handshake/trigger signals, see section 4.7.1.
24.	CLOCKB+	TTL, Variable Voltage or differential output of TS_CLKB.

25. GND or CLOCKB- Differential compliment of TS_CLKB or signal ground for TTL and Variable Voltage.
26. CH[97..112] I/O channels 97-112.
27. SIGMON-DRB1 Signal monitor for DRB1.
28. CH[113-128] I/O channels 113-128.
29. SIGMON-DRB2 Signal monitor for DRB2.
30. CH[129-144] I/O channels 129-144.
31. SIGMON-DRB3 Signal monitor for DRB3.
32. CH[145-160] I/O channels 145-160.
33. SIGMON-DRB4 Signal monitor for DRB4.
34. CH[161-176] I/O channels 161-176.
35. SIGMON-DRB5 Signal monitor for DRB5.
36. CH[177-192] I/O channels 177-192.
37. SIGMON-DRB6 Signal monitor for DRB6.

4.9 Error Logic

The error logic monitors the real time error and trigger signals from both timing modules.

Figure 4-11 shows the error logic of the SR192A.

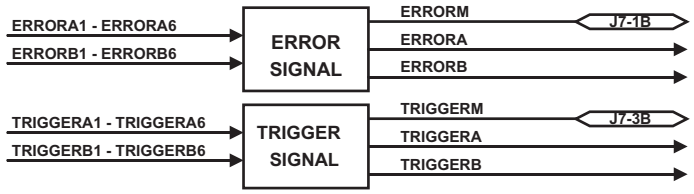

Figure 4-11 Error Logic Block Diagram

The following list describes the functional blocks shown in the figure above.

1. ERROR SIGNAL Logic that 'OR's the error signals from all the I/O modules and the J7 connector into separate error flags for TSA and TSB.
4. TRIGGER SIGNAL Logic that 'AND's the trigger signals from all the I/O modules and the J7 connector

The following list describes the signals shown in figure 4-11.

1. ERRORA1 - ERRORA6 Real time error flag from each TSA I/O module.
2. ERRORB1 - ERRORB6 Real time error flag from each TSB I/O module.
7. TRIGGERA1-TRIGGERA6 Real time trigger flag from each TSA I/O module.
8. TRIGGERB1-TRIGGERB6 Real time trigger flag from each TSB I/O module.
7. ERRORM Error flag (open collector 'OR') to/from the J7 master/slave connector.
8. ERRORA Error flag to the TSA timing module and error counter/RAM logic.
9. ERRORB Error flag to the TSB timing module.
15. TRIGGERM trigger flag (open collector 'AND') to/from the J7 master/slave connector.
16. TRIGGERA trigger flag to the TSA timing module.
17. TRIGGERB trigger flag to the TSB timing module..

4.9.1 Error Signal Generation

The error signals from both digital resources as well as the front panel master/slave connector (J7) can be programmed to generate a single error flag that can be tested. Table 4-1 illustrates how the error flags are generated.

SR192A Setting	ERRORA TRUE if	ERRORB TRUE if	ERRORM TRUE if
SR192A Independent, TSA/TSB not linked	Any ERRORA<n> signal true.	Any ERRORB<n> signal true.	N/A
SR192A Independent, TSA/TSB linked	Any ERRORA<n> or ERRORB<n> signal true.		N/A
SR192A Master/slave, TSA/TSB not linked	Any ERRORA<n> or ERRORM signal true.	Any ERRORB<n> signal true.	Any ERRORA<n> signal true.
SR192A Master/slave, TSA/TSB linked	Any ERRORA<n> or ERRORB<n> or ERRORM signal true.		Any ERRORA<n> or ERRORB<n> signal true.

Table 4-1 Error Signal Generation

4.9.2 Trigger Signal Generation

The trigger signals from both digital resources as well as the front panel master/slave connector (J7) can

be programmed to generate a single trigger flag that can be tested. Table 4-2 illustrates how the trigger flags are generated.

SR192A Setting	TRIGGERA TRUE if	TRIGGERB TRUE if	TRIGGERM TRUE if
SR192A Independent, TSA/TSB not linked	All TRIGGERA<n> signals true.	All TRIGGERB<n> signals true.	N/A
SR192A Independent, TSA/TSB linked	All TRIGGERA<n> and TRIGGERB<n> signals true.		N/A
SR192A Master/slave, TSA/TSB not linked	All TRIGGERA<n> and TRIGGERM signals true.	All TRIGGERB<n> signals true.	All TRIGGERA<n> signals true.
SR192A Master/slave, TSA/TSB linked	All TRIGGERA<n> and TRIGGERB<n> and TRIGGERM signals true.		All TRIGGERA<n> and TRIGGERB<n> signals true.

Table 4-2 Trigger Signal Generation

Appendix A Glossary of Terms

A16/A24/A32	The VXI address is segmented into three separate areas by a group of VXI signals called the address modifiers (AM0-AM5). These three areas are called A16, A24 and A32. Every VXI module is mapped into 64 bytes of the A16 memory. VXI modules, in addition, may request additional memory map space in the A24 or A32 space. The SR192A maps all the Timing and I/O modules registers into the A24/A32 space.
ADEL_CLK	Address Delay Clock. This signal, generated by the timing generator, clocks the response address delay register on the I/O modules.
CELL	A cell is a single element of a timing set. A timing set can have from 2 to 256 cells. 1 CELL = 1 period of TS_CLK.
CHANNEL TEST	Allows any channel of the installed I/O modules to be used as a test input (TEST1 or TEST2).
ERROR	Registered signal from the response comparator which indicates that the response data did not match the expect and mask data when the input strobe occurred.
FCNTL1/2	Front panel input signals (from the J8 connector) that can be selected to either enable stimulus or strobe response data.
FMA	Field Memory Address. This group of signals is generated by the word generator and broadcast to the I/O modules. The FMA directly selects the stimulus/response memory word.
FUNCTION CODE(FC)	Each module in a SR192A is assigned a 256K segment of the A32/A24 address map. The 256K can be split into sixteen unique areas via an additional four bits (F0-F3) which is routed to each module. The binary weighted value of the four signals generates sixteen function codes. Each module can define a single register for each function code or an array of 256K registers. Appendix B lists the function codes for this module.
HALF PHASE TIMING	The ability to generate signals that are one-half the period of the TS_CLK. Typically used to enhance the performance of serial operations or to format output data.
HANDSHAKE	Process used to synchronize data to/from a UUT utilizing SR101A timing module test inputs and timing outputs.
I/O CHANNELS	Sixteen bi-directional data channels available per I/O module slot.
I/O MODULE	Any of Talon's Stimulus/Response modules for the SR192A.
JEN	JUMP ENABLE enables a jump condition on one or more words of a table.
JUMP	A "jump" occurring during the execution of a step causes the execution of this step to cease and the execution of another sequence step to begin.
LINKED MODE	TSA and TSB operating synchronously.
MA_INC	The memory address (FMA) is always incremented at start of each timing cycle (First Cell). The "MA_INC" signal may be used to increment the FMA in later timing cells. The FMA will be incremented at the beginning of the next cell after the

	"MA_INC". "MA_INC" can be programmed in every other cell except the last two cells.
MODE_EN	Controls the execution of the "Serial", "Multiplex" or "Increment" I/O modes. The MODE_EN source may be one of the TSES1-6 signals, FCNTL1, FCNTL2 or none
.MASTER MODE	Two or more SR192A's operating synchronously.
OUTPUT ENABLE	Enable signal. This signal can be used to enable a group of I/O channels. The source of output enable can be a TSES1-6 signal, FCNTL1 or FCNTL2. The enable signal can also be set to "Always" or "Never".
RECORD STROBE	The record strobe latches the "RECORD ADDR" in the "RESPONSE ADDRESS LOGIC" and then generates the write pulse to the record memory.
RESPONSE	The response data of the SR192A is comprised of EXPECT, MASK and RECORD memories.
RESPONSE STROBE	This signal registers the Expect, Mask and response data into the compare register and initiates the real time compare.
SADDR	The selected address from either the VXI Backplane or the CPU.
SCPI	Standard Commands for Programmable Instruments.
SDATA	The selected data bus from either the VXI Backplane or the CPU.
SEQUENCE	A sequence is an ordered list of stimulus/response actions consisting of one or more sequence steps.
SEQUENCE STEP	A sequence step is a single element of a sequence. A sequence step selects a timing set, table, loop count, jump condition and control flags.
SHIFT STROBE	This signal is used to sample intermediate data for the serial or multiplex mode.
STIM_LOAD	Timing module control signal that loads the data from the stimulus memory into the output registers. The rising edge of this control signal also registers the stimulus address (FMA) when the output register delay is enabled. The falling edge performs the Data Format function if enabled.
STIMULUS	The stimulus data of the SR192A is determined by the OUTPUT and TRISTATE memory data, output enables, output mode and output format.
TABLE	A table is a defined number of STIMULUS/RESPONSE words. It is located within a specific range of FMA addresses. The FMA range is broadcast to all the I/O modules connected to the timing module.
TEST1, 2	Two test inputs that can be selected from the TSINPUTs, CHANTEST signals or TRIGGER.
TIMING MODULE	An SR192A plug-in module that controls stimulus/response timing and sequencing.
TIMING SET	A timing set is the structure that is created that defines the stimulus/response timing. Sixteen timing sets can be defined of 2-256 cells.
TRANSFER	See WORD.

TS_CLK	Timing Set Clock. This signal clocks the timing generator. Each cell is one period of the TS_CLK.
TSES1...6	General purpose Timing Set signals that can be used to enable stimulus drivers, enable mode functions, strobe data into registers or strobe response data into memory.
TSINPUT1/2	Front panel test input signal. Each timing module has two test input signals available, TEST1 and TEST2. Either TSINPUT signal may be routed to TEST1 or TEST2 for Timing Set or Sequence Control.
TSINPUTM	The TSINPUT1A signal which is synchronized by the clock and used in Linked or Master/Slave operations.
TSIO	Timing Set Input Output - One of two available modules used to translate timing module signals.
TSOUT1..5	Timing Set Output One through Five. General purpose output signals generated by the timing module.
UUT	Unit Under Test
VECTOR	A collection of up to four input channels whose High/Low states define a vector with up to sixteen values (one value for each combination of the input levels).
VECTOR BUS	The vector bus is an intermodule bus that connects all of the Series A I/O modules with the associated timing module(s). This bus allows the user to route any channel input to any of the four vector bus lines. The Timing Module allows the user to jump to a sequence address where the four vector bus signals address a LUT to determine the jump address.
VEN	VECTOR ENABLE enables a jump condition which has a JEN to jump to a sequence based on a vector value generated by the I/O modules.
VXI	VMEbus Extensions for Instrumentation.
WORD	A word is a single element of a table. The width of a word depends on the number and type of I/O modules installed in the SR192A.

Appendix B Address Map

SR192A addressing is split into two sections, A16 and A24/A32. The two sections are selected by six signals on the VXI backplane called the address modifiers.

The SR192A will respond to the following A16 address modifier settings: hex 29 and 2D.

If the SR192A is set to A24 addressing (section 3.2.3.2) then it will respond to the following address modifier settings: hex 39, 3A, 3B, 3D, 3E and 3F.

If the SR192A is set to A32 addressing (section 3.2.3.2) then it will respond to the following address modifier settings: hex 39, 3A, 3B, 3D, 3E and 3F.

1 A16 Map

The A16 registers and their function are defined by the VXI standard.

Register	Offset	R/W	Description
ID	0x0	read	Instrument ID Register
LA	0x0	write	Logical Address Register
DEVICE	0x2	read	Device Register
STATUS	0x4	read	Status Register
CONTROL	0x4	write	Control Register
OFFSET	0x6	read/write	A32/A24 Offset Register
PROTOCOL	0x8	read	Protocol Register
RESPONSE	0xA	read	Response Register
DATA LOW	0xE	read/write	Data Low

Table B-1 A16 Address Map

The following sections describes the registers listed above.

1.1 ID Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Device Class		Address Space		Manufacturer ID											

Field/Bit Description:

Device Class	Specifies the VXI device classification: SR192A = hex 2 (message based).
Address Space	Device address mode; SR192A = hex 1 (A16/A32) or hex 0 (A16/A24) based on the CPU switch setting, see section .3.2.3.2
Manufacturer ID	Unique ID; Talon Instruments = hex 909.

1.2 LA Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Logical Address															

Field/Bit Description:

Logical Address	Specifies the logical address if dynamic configuration is enabled, see section 3.2.3.1.

1.3 Device Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Required Memory				Device Type											

Field/Bit Description:

Required Memory	Specifies the amount of A24/A32 memory addressing required; SR192A = 8388K
Device Type	Unique device identifier; SR192A = hex 103.

1.4 Status Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A24/A32 Active	MODID	NU										Ready	Passed	NU	

Field/Bit Description:

A24/A32 Active	Indicates whether the A24/A32 memory space is enabled (1) or disabled (0).
MODID	A zero in this field indicates that the SR192A is selected by a high state on the P2 MODID line.
Ready	A zero in this field indicates that the SR192A is still in the self test/initialize state during power up. A one in this field with a zero in the “passed” field indicates the SR192A failed register initialization. A one in this field along with a one in the “passed“ field indicates the SR192A is operational.
Passed	A zero in this field indicates the SR192A is either executing or has failed self test. A one indicates the SR192A has passed self test and is ready for operation.

1.5 Control Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A24/A32 Enable	NU													Sysfail Inhibit	Reset

Field/Bit Description:

A24/A32 Enable	A one (1) enables access to the A24/A32 registers of the SR192A. A zero (0) disables access.
Sysfail Inhibit	A one (1) in this field disables the SR192A from driving the SYSFAIL line.
Reset	A one (1) in this field forces the SR192A into the reset state.

1.6 Offset Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A24 MSA	NU														
A32 MSA									NU						

Field/Bit Description:

A24 MSA	This bit is mapped to the most significant bit of the A24 address decoder.
A32 MSA	These 9 bits are mapped to the upper 9 bits of the A32 address decoder.

1.7 Protocol Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMDR	Signal Register	Master	Interrupter	FHS	Shared Memory	Reserved						NU			

Field/Bit Description:

CMDR	Always 1, this field indicates that the SR192A is a servant only.
Signal Register	Always 1, this field indicates that the SR192A does not have a signal register.
Master	Always 1, this field indicates that the SR192A does not have VMEbus Master capability.
Interrupter	Always 1, this field indicates that the SR192A has interrupter capability.
FHS	Always 1, this field indicates that the SR192A supports the normal transfer mode.
Shared Memory	Always 1, this field indicates that the SR192A does not support the shared memory protocol.
Reserved	All ones (hex 3F) will be returned.

1.8 Response Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Reserved	DOR	DIR	Err	Read Ready	Write Ready	NU								

Field/Bit Description:

Bit 15	Always zero (0)
Reserved	Always one (1)
DOR	Data Output Ready; A one (1) in this field indicates that the SR192A is ready to output data to the commander using the byte transfer protocol.
DIR	Data Input Ready; A one indicates that the SR192A is ready to accept data from the commander using the byte transfer protocol.
Err	A zero (0) indicates that a word serial error has occurred.
Read Ready	A one (1) indicates that the SR192A's DATA LOW register contains data to be read.
Write Ready	A one (1) indicates that the SR192A is ready for data to be written to the DATA LOW register.

1.9 DATA LOW Register

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Command/Data															

Field/Bit Description:

Command/Data	Commands and data are passed between the SR192A and the commander by reads and writes to this register.

2 A32 Map

The SR192A requests approximately 8M of address memory from the resource manager on power up. This address memory allows the SR192A user to directly access the stimulus/response memory as well as control/status registers.

The 8M of address memory is segmented into sections listed below.. Along with the module decodes

Section	Base Address	Function Code	Description	Section
SYSTEM	0	0-4	System Memory	2.1
STATUS/CONTROL	40000	NU	VXI A32 Decodes,	2.2
MFC	70000	0-F	DAC/MFC Module	2.3
PROBE	C0000	NU	Probe GOOD0/GOOD1	2.5
TSA	100000	0-F	Timing Set A Module	2.6
TSB	180000	0-F	Timing Set B Module	2.6
DRA1	200000	0-F	Driver/Receiver Module	2.7
DRA2	280000	0-F	Driver/Receiver Module	2.7
DRA3	300000	0-F	Driver/Receiver Module	2.7
DRA4	380000	0-F	Driver/Receiver Module	2.7
DRA5	400000	0-F	Driver/Receiver Module	2.7
DRA6	480000	0-F	Driver/Receiver Module	2.7
DRB1	500000	0-F	Driver/Receiver Module	2.7
DRB2	580000	0-F	Driver/Receiver Module	2.7
DRB3	600000	0-F	Driver/Receiver Module	2.7
DRB4	680000	0-F	Driver/Receiver Module	2.7
DRB5	700000	0-F	Driver/Receiver Module	2.7
DRB6	780000	0-F	Driver/Receiver Module	2.7

Table B-2 SR192A A24/A32 Section Map

Each section can be further divided into sixteen pages using four function code signals (F0 through F3) to generate a function code.

Function code 15 (FC15) for each of the module sections is used to identify the module type. ID's 0 - 7 are reserved for MFC modules, 8 - 15 are reserved for timing modules and 16 - 128 are reserved for I/O modules.

The following sections describe each A24/A32 section listed above.

2.1 SYSTEM MEMORY

The SR192A System Memory is comprised of up to 5 banks of memory located at address 0-0x3FFFF. Each bank is addressed using the function code bits.

Commands are available to do the following functions:

1. Restart using upper RAM1 as new system.
2. Reprogram flash RAMs using the data in upper RAM1.

Function Code Assignments:

FC0 Read Flash RAM (contains the system firmware).

FC1 Read/write bank one RAM. This bank can be swapped with flash for firmware updates.

FC2 Read/write bank 2 RAM.

FC3 Read/write bank 3 RAM.

FC4 Read/write bank 4 RAM.

2.2 Status/Control

The SR192A A24/A32 status/control registers are listed below.

Register	Offset	R/W	Register Description
WSEXCLK	0x40000	write	Programs external clock source, master mode and error memory address mode.
WRTMRST	0x40002	write	Clear error counter, reset timing module error and time-out
RDTMSTA	0x40002	read	Timing module status register
ERREG	0x40006	write	Error Control Register
DRVRRD	0x40008	read	Variable Voltage Driver Status Register
VXIFC	0x40010	write	VXI Function Code Register
TTLTRG-	0x40012	write	TTLTRG Control Register

Table B-3 A24/A32 Status/Control Registers

2.2.1 WSEXCLK (0x40000)

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Factory Reserved (must program high)							Master Enable	NU		EXCLKM source		EXCLK-TSB source		EXCLK-TSA, ICLKM source	

Bit Description:

Bit 0 and 1 selects the EXCLK-TSA source when the SR192A is not in the master mode. If the SR192A is in the master mode then bit 0 and 1 selects the internal clock source of EXCLKM. ICLKM = master bus clock source.

Bit 1	Bit 0	Master Mode	EXCLK-TSA
X	X	ON	EXCLKM
0	0	OFF	EXCLK1
0	1	OFF	EXCLK2
1	0	OFF	EXCLKM
1	1	OFF	PGMCLK

Bit 1	Bit 0	Master Mode	ICLKM
X	X	OFF	N/A
0	0	ON	TSACLK
0	1	ON	TSACLK
1	0	ON	TSACLK
1	1	ON	PGMCLK

Bit 2 and 3 selects the EXCLK-TSB source.

Bit 3	Bit 2	EXCLK-TSB
0	0	EXCLK1
0	1	EXCLK2
1	0	EXCLKM
1	1	PGMCLK

Bit 4 and 5 selects the EXCLKM source.

Bit 5	Bit 4	EXCLKM
0	0	EXCLK1
0	1	EXCLK2
1	X	ICLKM

Bit 8 enables the master mode.

Bit 8	Master Mode
0	ON
1	OFF

Bits 9 through 15 are factory reserved and must be programmed high.

2.2.2 WRTMRST (0x40002)

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used												Reset TSB timeout	Reset TSA timeout	Reset TSB halt	Reset TSA halt

Bit 0 clears the TSA halt LED.

Bit 0	TSA halt LED
0	OFF
1	No change

Bit 1 clears the TSB halt LED.

Bit 1	TSB halt LED
0	OFF
1	No change

Bit 2 clears the TSA timeout LED.

Bit 2	TSA timeout LED
0	OFF
1	No change

Bit 3 clears the TSB timeout LED.

Bit 3	TSB timeout LED
0	OFF
1	No change

2.2.3 RDTMSTA (0x40002)

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU		TSB timing module status						NU		TSA timing module status					

Bit definitions:

Bit #	Level	TSA Status
0 IDLE-	High (1)	TSA in reset state
	Low (0)	TSA in idle or run state, see bit 1.
1 RUN-	High (1)	TSA not running, idle or reset.
	Low (0)	TSA running.
2 WAIT-	High (1)	TSA not waiting for input trigger/handshake.
	Low (0)	TSA waiting for input trigger/handshake.
3 TIMEOUT	High (1)	TSA input trigger/handshake timed out.
	Low (0)	No TSA timeout.
4 HALT	High (1)	TSA halt on error occurred.
	Low (0)	No TSA halt.
5 COMPARE	High (1)	TSA waiting for compare.
	Low (0)	TSA not waiting for compare.

Bit #	Level	TSB Status
0 IDLE-	High (1)	TSB in reset state
	Low (0)	TSB in idle or run state, see bit 1.
1 RUN-	High (1)	TSB not running, idle or reset.
	Low (0)	TSB running.
2 WAIT-	High (1)	TSB not waiting for input trigger/handshake.
	Low (0)	TSB waiting for input trigger/handshake.
3 TIMEOUT	High (1)	TSB input trigger/handshake timed out.
	Low (0)	No TSB timeout.
4 HALT	High (1)	TSB halt on error occurred.
	Low (0)	No TSB halt.
5 COMPARE	High (1)	TSB waiting for compare.
	Low (0)	TSB not waiting for compare.

2.2.4 ERREG (0x40006)

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU									TSIO DRVFLT irq mask	Timing channel enable	TSIO DRVFLT reset	TRIGGER source		ERROR source	

Bit definitions:

Bit 0 and 1 selects the error flag source.

Bit 1	Bit 0	ERRORA Source	ERRORB Source	ERRORM Source
0	0	DRA1-DRA6	DRB1-DRB6	NONE
0	1	DRA1-DRB6	DRA1-DRB6	NONE
1	0	DRA1-DRB6,ERRORM	DRA1-DRB6,ERRORM	DRA1-DRB6
1	1	DRA1-DRA6,ERRORM	DRB1-DRB6	DRA1-DRA6

Bit 2 and 3 selects the error flag source.

Bit 3	Bit 2	TRIGGERA Source	TRIGGERB Source	TRIGGERM Source
0	0	DRA1-DRA6	DRB1-DRB6	NONE
0	1	DRA1-DRB6	DRA1-DRB6	NONE
1	0	DRA1-DRB6,COMPAREM	DRA1-DRB6,TRIGGERM	DRA1-DRB6
1	1	DRA1-DRA6,TRIGGERM	DRB1-DRB6	DRA1-DRA6

Bit 4 clears the TSIO drive fault flag.

Bit 4	TSIO DRVFLT
0	Set TSIO drive fault flag.
1	Reset TSIO drive fault flag.

Bit 5 enables/disables the drivers for TSOUTA1-TSOUTA5, TSOUTB1-TSOUTB5, and CLOCKA.

Bit 5	Output Drivers
0	Enabled.
1	Disabled.

Bit 6 masks the tsio drive fault flag (TSIO DRVFLT).

Bit 6	TSIO DRVFLT Irq Mask
0	Enable TSIO drive fault irq.
1	Disable TSIO drive fault irq.

2.2.5 DRVRRD (0x40008)

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								TSIO DRVFLT flag	TSIO DRVFLT irq mask	DRVFLT flag	OVERDRIVE LED	NU			

Bit definitions:

Bits 4 through 7 return the Variable Voltage driver status.

Bit #	Level	Description
4	High (1)	OVERDRIVE LED off.
	Low (0)	OVERDRIVE LED on.
5	High (1)	I/O and TSIO driver fault flag false.
	Low (0)	I/O or TSIO driver fault flag true.
6	High (1)	TSIO driver fault irq mask enabled.
	Low (0)	TSIO driver fault irq mask disabled.
7	High (1)	TSIO driver fault false.
	Low (0)	TSIO driver fault true.

2.2.6 VXIFC (0x40010)

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU												Function Code			

Bit definitions:

Bit 0 through 3 sets the function code value.

Bit 3	Bit 2	Bit 1	Bit 0	Function Code
0	0	0	0	FC0
0	0	0	1	FC1
0	0	1	0	FC2
0	0	1	1	FC3
0	1	0	0	FC4
0	1	0	1	FC5
0	1	1	0	FC6
0	1	1	1	FC7
1	0	0	0	FC8
1	0	0	1	FC9
1	0	1	0	FC10
1	0	1	1	FC11
1	1	0	0	FC12
1	1	0	1	FC13
1	1	1	0	FC14
1	1	1	1	FC15

2.2.7 TTLTRG (0x40012)

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								TTLTRG input enable	TTLTRG input select			TTLTRG output enable	TTLTRG output select		

Bit definitions:

Bit 0, 1 and 2 selects the TTLTRG output selection.

Bit 2	Bit 1	Bit 0	TTLTGR Selection
0	0	0	TTLTRG0
0	0	1	TTLTRG1
0	1	0	TTLTRG2
0	1	1	TTLTRG3
1	0	0	TTLTRG4
1	0	1	TTLTRG5
1	1	0	TTLTRG6
1	1	1	TTLTRG7

Bit 3 enables/disables the output TTLTRG driver.

Bit 3	TTLTRG Output Driver
0	OFF
1	ON

Bit 4, 5 and 6 selects the TTLTRG input selection.

Bit 6	Bit 5	Bit 4	TTLTGR Selection
0	0	0	TTLTRG0
0	0	1	TTLTRG1
0	1	0	TTLTRG2
0	1	1	TTLTRG3
1	0	0	TTLTRG4
1	0	1	TTLTRG5
1	1	0	TTLTRG6
1	1	1	TTLTRG7

Bit 7 enables/disables the input TTLTRG receiver.

Bit 7	TTLTRG Input Receiver
0	OFF
1	ON

2.3 MFC

Refer to the specific reference manual of the module installed in the DAC/MFC slot.

2.4 PROBE

See the SR210 reference manual.

2.5 TSA/TSB

Refer to the specific timing module reference manual.

2.6 DRAn/DRBn

Refer to the specific I/O module reference manual.