

REFERENCE MANUAL

SR127A

8-Channel ECL Differential
Stimulus/Response Module

Manual Revision: 09/21/06
Manual Part Number: SRMM924
Instrument Part Number: SR127A

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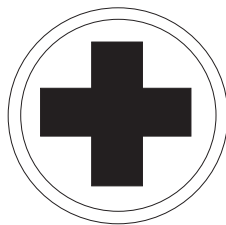
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- Pay attention to the **CAUTION** statements. They point out situations that can prevent proper operation.
- Use ESD static control procedures when handling the SR192A or any of its modules.

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1 Introduction

Talon's SR192A digital test module is a modular VXI stimulus/response system. The SR192A baseboard is a two slot, "C" size module which houses up to 12 I/O modules. I/O modules are designed to provide either 8/16 stimulus/response channels for a total of 96 or 192 channels. Modules provide many logic options such as fixed voltage TTL, RS485/422, ECL or variable voltages of +7/-5V.

Multiple SR192A's may be linked in a master/slave configuration to provide up to 1152 channels in a single VXI 13-slot chassis. Contact Talon for details on this type of configuration.

This manual is for the SR127A I/O module. The SR127A is an 8 channel, dynamic module with selectable double ended ECL drivers/receivers. Each SR127A has a single 8 channel group allowing up to 12 groups in a single SR192A. The eight I/O channels are uni-directional using a tristate memory to control direction on a per nibble basis. The output enable and input strobe signals are assigned in groups of eight channels.

The SR127A utilizes a five memory architecture, OUTPUT, TRISTATE, EXPECT, MASK and RECORD. This architecture allows the user to perform real-time error detection and recording. Each memory is 256K bits per channel.

The SR127A is a multi-function I/O module. Talon's multi-function I/O modules provide several operating modes in addition to the standard parallel stimulus/response operation. Each 8 channel group may be assigned the same or a different mode from other groups. These special operating modes are:

Multiplex	This mode allows the user to program any number of eight channel groups (or all groups) to operate with double the memory and twice the data rate.
Serial	This mode allows the user to send and receive data through a single channel of the eight channel group. Data is input through the MSB and output through the LSB. Adjacent eight channel groups may be linked to provide for 16, 24, etc., bit words. This mode provides the user with the ability to easily emulate serial busses as well as increasing the memory depth.
Increment	This mode provides an increment function that operates on the data stored in the output register. Using this mode a user can easily generate incremented data such as addresses for RAM or ROM testing without using I/O memory. The eight channel groups may be linked to provide wider data words.

All operating modes may output formatted or unformatted data. Formats available are RTO, RTC, RTZ, RTT and HOLD, see Section 4.1.6.3.

The layout of this manual is in five sections described below:

1. Introduction	This section.
2. Specifications	Electrical and environmental specifications of the SR127A.
3. Jumpers/Installation	Description of the jumpers and installation of the SR127A.
4. Functional Description	Functional description of the SR127A hardware.
5. Memory Data Mapping	Memory to channel mapping

In addition two Appendices are included:

A. Glossary of Terms	Definition of terms used in this manual.
B. Function Code Map	Hardware register description.

2 Specifications

The following sections list the specifications of the SR127A I/O module.

2.1 I/O Module

Number of Channels	
Differential Pairs	8
Number of Stimulus Memories	2
OUTPUT, TRISTATE	
Number of Response Memories	3
EXPECT, MASK, RECORD	
Data Format Channel Modes	
Non Return	HOLD
Return to Zero	RTZ
Return to One	RTO
Return to Compliment	RTC
Return to Tristate	RTT
Increment Channel Mode	Increment 1- 65,536
Data Shift Channel Modes	
Shift by one	SERIAL
Shift by eight	MULTIPLEX
Memory Depth per Channel	
Standard and Increment Modes	262144
Multiplex Mode	524288
Serial Mode	4194303
Maximum Stimulus Data Rate	50 MHz
Output Enable Source (common to all channels)	10
Internal (TSES1-6, ALWAYS, NEVER)	8
External (FCNTL1, FCNTL2)	2
Internal Output Enable Resolution	½ TS_CLK
Output Enable Placement (common to all channels)	0-20ns with 1ns increments
Maximum Response Data Rate TTL	50 MHz
Response Strobe Source (common to all channels)	8
Internal (TSES1-6)	6
External (FCNTL1, FCNTL2)	2
Internal Response Strobe Resolution (common to all channels)	½ TS_CLK
Response Strobe Placement (common to all channels)	0-20ns with 1ns increments
Record Address Strobe Source (common to all channels)	8
Internal (TSES1-6)	6
External (FCNTL1, FCNTL2)	2
Internal Record Address Strobe Resolution (common to all channels)	½ TS_CLK
Record Address Strobe Placement (common to all channels)	0-20ns with 1ns increments
Shift Strobe Source (MULTIPLEX/SERIAL mode) (common to all channels)	8
Internal (TSES1-6)	6
External (FCNTL1, FCNTL2)	2
Internal Shift Strobe Resolution (common to all channels)	½ TS_CLK
Shift Strobe Placement (common to all channels)	0-20ns with 1ns increments
Output Driver/Input Receiver	100H680

2.2 Electrical

The following lists the differential driver/receiver electrical characteristics.

High Level Output Voltage (loaded 51 Ω to -2V)	-1.1V min
Low Level Output Voltage (loaded 51 Ω to -2V)	-2.0V max
High Level Source Current	80 mA max
Tri-States Output Voltage (both outputs of each channel)	-2.0 V typ
Input Tri-State Detect (generates a "true" response) both inputs	<-1.5V typ
High Level Input Threshold	-1.13V max
Low Level Input Threshold	-1.48V min
Input/Output Termination (factory default)	51 Ω to -2V

2.3 Timing Characteristics

The SR127A is a module that operates within the SR192A system. Refer to the SR192A Timing Reference Manual for the timing characteristics of the SR192A system.

2.4 Environmental

Temperature Range

Operating0°C to +50°C
 Storage-40°C to +71°C (RH not controlled)

Altitude

OperatingSea level to 10,000 ft.
 StorageSea level to 40,000 ft.

Relative Humidity (non condensing)

0°C to +10°Cnot controlled
 +11°C to +30°C95+/-5%RH
 +31°C to +40°C75+/-5%RH
 +41°C to +50°C45+/-5%RH

2.5 Size

Dimension

4.93 cm x 22.61 cm (1.94" x 8.9")

Weight

0.074 kg (2.6 oz)

2.6 Power Requirements

The power requirements listed in table 2-1 are for a single SR127A with the drivers unloaded.

Voltage	Peak Current	Dynamic Current	Note
+5V	0.564A	TBD	-
-5.2V	0.379	TBD	-
-2V	0	0	-
+12V	0	0	-
-12V	0	0	-
+24V	0	0	-
-24V	0	0	-
V+	0	0	-
V-	0	0	-

Table 2-1 SR127A Voltage Requirements

3 Jumpers/Installation

The SR127A I/O module requires firmware revision 1.09 or later for proper operation. Contact Talon Instruments for information on firmware upgrades.

Figure 3-1 below is a locator diagram for test points and jumpers located on the SR127A.

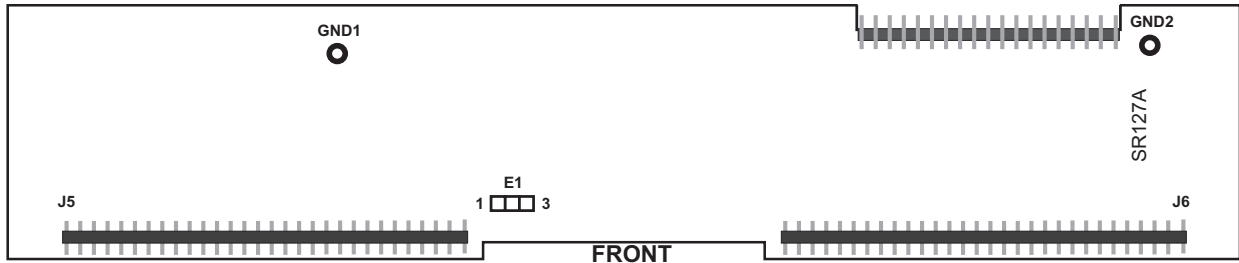


Figure 3-1 Test Point/Jumper Locations

3.1 Test Point Description

Table 3-1 describes the test points on the SR127A I/O module.

Test Point	Mnemonic	Description
TP1	GND1	Signal Ground
TP2	GND2	Signal Ground

Table 3-1 SR127A Test Point Description

3.2 Jumper Description

The SR127A has a single jumper (E1) that is used to select the driver/receiver termination voltage.

- E1-1 to E1-2 -5.2V termination.
- E1-2 to E1-3 -2V termination (factory default).

3.3 Installation

Each SR192A baseboard can house up to 12 I/O modules. I/O modules are installed in baseboard slots DRA1 through DRA6 and DRB1 through DRB6, see Figure 3-2.

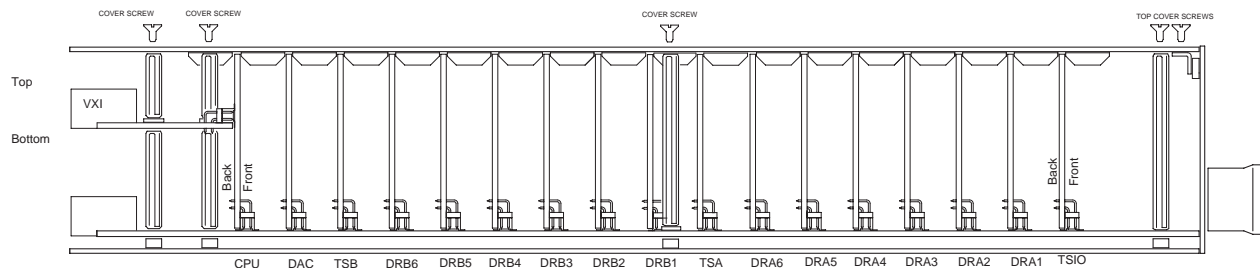


Figure 3-2 SR192A Baseboard Side View

The SR192A Series includes an intermodule bus board(s) across the top of the I/O modules and the timing modules to provide an interconnect path. The front intermodule bus board (P/N 20580-001) has resistors installed in positions R1, R2 and R3. The rear intermodule module bus board (P/N 20580-002) has

resistors installed in positions R7, R8 and R9, see Figure 3-4. If only one timing module is installed then 20580-002 must be installed in the front position.

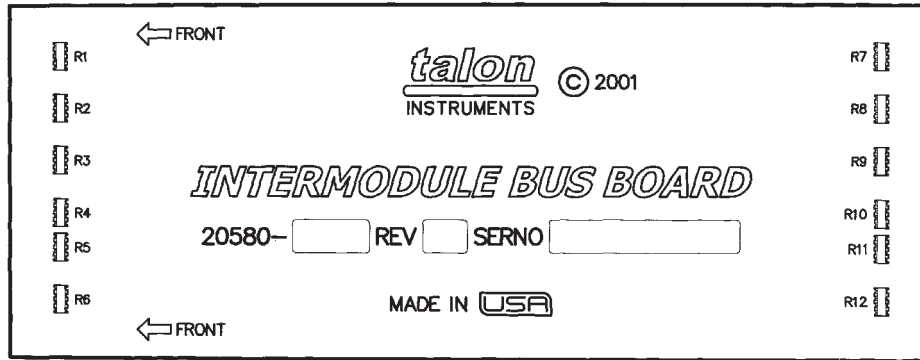


Figure 3-4 Intermodule Bus Board

The intermodule Bus Boards are installed as illustrated in Figure 3-3.

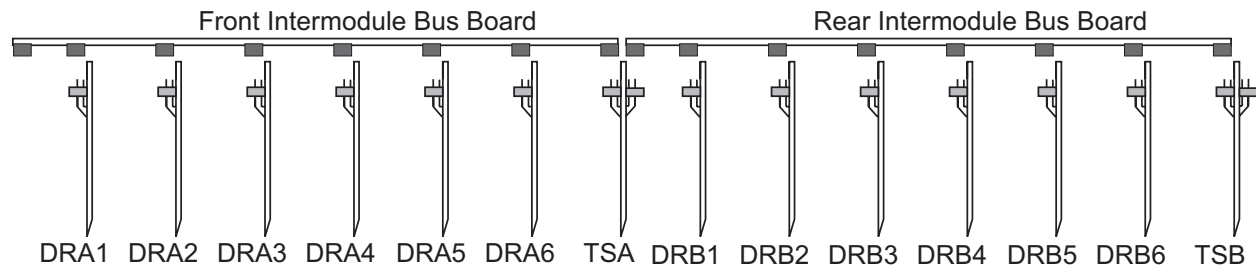


Figure 3-3 Intermodule Board Installation

Perform the following steps to add or replace an I/O module:

- Step 1. Using ESD protocols remove the SR192A from the VXI chassis.
- Step 2. Remove the top cover screws, refer to Figure 3-2.
- Step 3. Remove the Intermodule Bus Board(s) connecting any I/O modules and timing set modules that are to be replaced.
- Step 4. If replacing an I/O module, remove it by grasping at each corner and gently rocking forward and back while pulling it away from the baseboard.
- Step 5. Insert the I/O module in the desired DRA or DRB module slot, refer to figure 3-2, by lining up the J1 and J2 connectors with the baseboard connectors and gently pushing down. All SR192A modules are keyed along the associated mating connector. If the module cannot be inserted, make sure you are inserting the module into the correct slot, check for bent pins and make certain the pins are aligned with the mating connector on the baseboard.
- Step 6. Reinstall the Intermodule Bus Board(s). The front board overhangs by one connector (see Figure 3-3), the module installed in DRA1 (ascertain the bus board connectors are all aligned and gently press downward).

CAUTION
Although the modules and the associated mating connectors have been keyed, it is possible to force a module into an incorrect slot.

4 Functional Description

The SR127A, along with all the other I/O modules, is controlled through the SR192A timing modules. Control signals are generated by the timing module which allow the SR127A to output stimulus data and record response data while the timing module is running. When the timing module is not running, the CPU module or VXI controller can program or query the stimulus/response memories on the SR127A. Figure 4-1 depicts the SR127A signal relationship to other components of the SR192A.

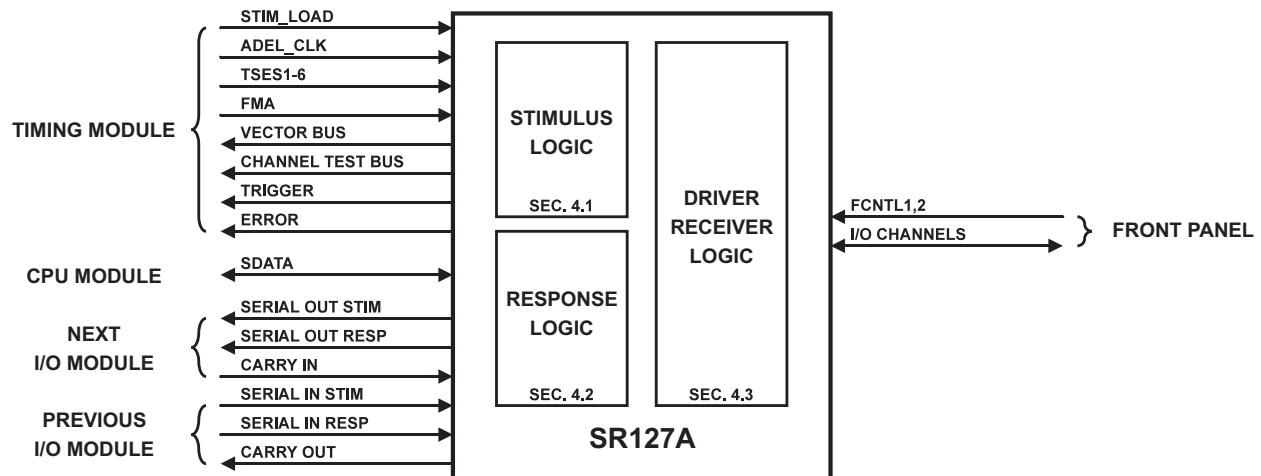


Figure 4-1 SR127A Signal Diagram

The following list describes the functional blocks shown in figure 4-1.

- | | | |
|----|-----------------------|--|
| 1. | STIMULUS LOGIC | The memories, registers and control bits that generate UUT input data. |
| 2. | RESPONSE LOGIC | The memories, registers and control bits that record UUT output data. |
| 3. | DRIVER/RECEIVER LOGIC | The driver/receiver ICs and terminators that connect the STIMULUS/RESPONSE logic to the UUT. |

The following list describes the signals shown in figure 4-1.

- | | | |
|-----|------------------|--|
| 1. | STIM_LOAD | Timing set signal used to control the stimulus logic. |
| 2. | ADEL_CLK | Timing set signal generated to delay the response record window. |
| 3. | TSES1-6 | Timing set signals used to control the stimulus/response logic. |
| 4. | FMA | Field Memory Address. While running the FMA is generated by the timing module and broadcast to all the I/O modules to select a new stimulus word. While not running the FMA is either the baseboard CPU or VXI address bus used to program/query the SR127A. |
| 5. | VECTOR BUS | Any four of the eight I/O channels can provide a 4-bit vector word used by the timing module to select a new timing sequence. |
| 6. | CHANNEL TEST BUS | Any two of the eight I/O channels can be used as a test input signal for the timing module handshake logic. |
| 7. | TRIGGER | Registered signal from the trigger and trigger mask register response comparator which indicates that the current response data matches. |
| 8. | ERROR | Registered signal from the response comparator which indicates that the response data did not match the expect and mask data when the input strobe occurred. |
| 9. | SDATA | Either the baseboard CPU or VXI data bus used to program/query the SR127A. |
| 10. | SERIAL OUT STIM | Serial stimulus signals (output and tristate data) to adjacent lower I/O module for SERIAL mode. |
| 11. | SERIAL OUT RESP | Serial response signal (receiver data) to adjacent lower I/O module for SERIAL mode. |
| 12. | CARRY IN | Carry input signal from adjacent lower I/O module for INCREMENT mode. |
| 13. | SERIAL IN STIM | Serial stimulus signals (output and tristate) from adjacent higher I/O module for SERIAL mode. |
| 14. | SERIAL IN RESP | Serial response signal (receiver data) from adjacent higher I/O module for SERIAL mode. |

- | | |
|------------------|---|
| 15. CARRY OUT | Carry output signal to adjacent higher I/O module for INCREMENT mode. |
| 16. FCNTL1,2 | Front panel signals used to control the stimulus/response logic. |
| 17. I/O CHANNELS | Eight bi-directional differential or single ended TTL channels. |

The following sections describe the three major logic elements of the SR127A (Stimulus, Response and Driver/Receiver).

4.1 Stimulus Logic

Figure 4-2 shows the stimulus logic block diagram.

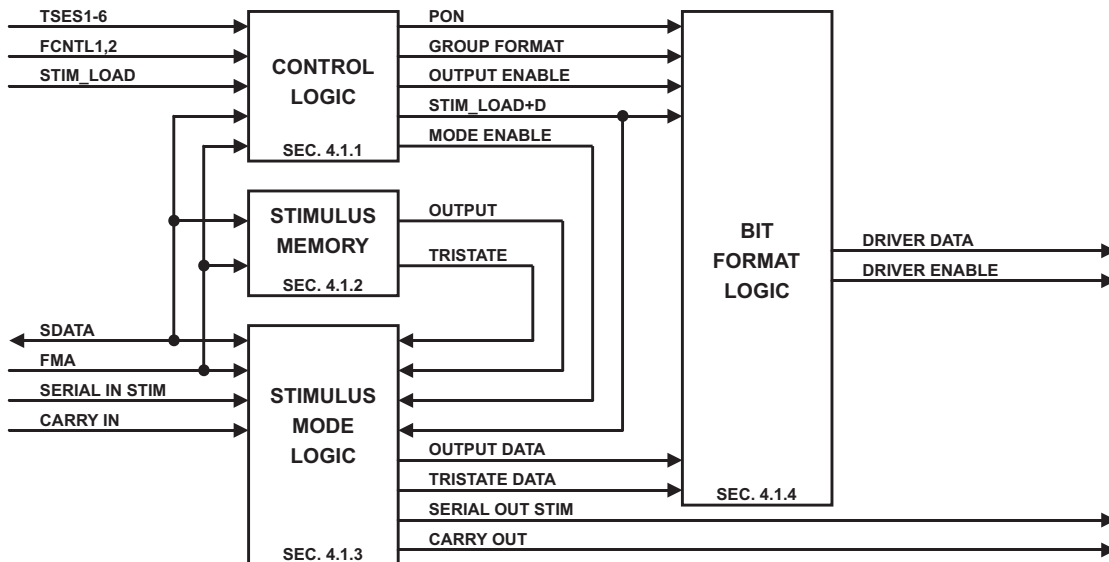


Figure 4-2 Stimulus Logic Block Diagram

The following list describes the functional blocks of figure 4-2.

- | | |
|---------------------|---|
| 1. CONTROL LOGIC | Used to select the output enable signal, mode enable signal and bit format selection. The output enable can also be delayed up to 20ns in 1ns increments. |
| 2. STIMULUS MEMORY | Two 256K by 16 memories allows the operator to define the logic level and enable any of the eight drivers during an output word. |
| 3. MODE LOGIC | Hardware that processes the stimulus memory based on the selected I/O mode, standard, increment, serial multiplex or static. |
| 4. BIT FORMAT LOGIC | Performs the selected bit format on the output and tristate data and sends the result to the drivers. |

The following list describes the signals shown in figure 4-2.

- | | |
|-------------------|--|
| 1. TSES1-6 | Timing set signals that can be selected as either the "MODE ENABLE" or "OUTPUT ENABLE" by the user. |
| 2. FCNTL1,2 | Front panel signals that can be selected as either the "MODE ENABLE" or "OUTPUT ENABLE" by the user. |
| 3. STIM_LOAD | Timing set signal used to control the mode and bit format logic. |
| 4. SDATA | Either the baseboard CPU or VXI data bus used to program/query the SR127A. |
| 5. FMA | Field Memory Address. While running the FMA is generated by the timing module and broadcast to all the I/O modules to select a new stimulus word. While not running the FMA is either the baseboard CPU or VXI address bus used to program/query the SR127A. |
| 6. SERIAL IN STIM | Serial stimulus signals (output and tristate) from adjacent higher I/O module for SERIAL mode. |
| 7. CARRY IN | Carry input signal from adjacent lower I/O module for INCREMENT mode. |
| 8. PON | Driver power enable/disable control. |
| 9. GROUP FORMAT | Selected group bit format. |
| 10. OUTPUT ENABLE | This signal can be used to enable or disable the entire group of output drivers. |
| 11. STIM_LOAD+D | Delayed "STIM_LOAD" signal. |
| 12. MODE ENABLE | Control signal that enables the mode logic. |
| 13. OUTPUT | Stimulus output memory data addressed by FMA. |

14.	TRISTATE	Stimulus tristate memory data addressed by FMA.
15.	OUTPUT DATA	Processed "OUTPUT" data passed to the bit format logic.
16.	TRISTATE DATA	Processed "TRISTATE" data passed to the bit format logic.
17.	SERIAL OUT STIM	Serial stimulus signals (output and tristate data) to adjacent lower I/O module for SERIAL mode.
18.	CARRY OUT	Carry output signal to adjacent higher I/O module for INCREMENT mode.
19.	DRIVER DATA	Data to the output drivers.
20.	DRIVER ENABLE	Enable to the output drivers.

4.1.1 Control Logic

The control logic allows the user to program the PON setting, GROUP FORMAT, OUTPUT ENABLE source and delay, STIM_LOAD delay and MODE ENABLE source.

4.1.1.1 PON Setting

The PON setting is used to enable/disable all the output drivers on the SR127A. See table 4-1 for a description of the effects of the PON setting to the driver outputs.

4.1.1.2 Group Format

The group format allows the user to select one of five bit formats or none to apply to the output data:

1. None - (Output registers disabled in standard mode with this format)
2. RTT - Return to Tristate
3. RTZ - Return to Zero
4. RTO - Return to One
5. RTC - Return to Compliment
6. HOLD - Keep current data

See section 4.1.4 for the bit format timing and control.

4.1.1.3 OUTPUT ENABLE Source and Delay

This logic allows the user to select the "OUTPUT ENABLE" signal for the lower group. The selected signal can be delayed from 0 to 20ns in 1ns increments.

1. TSES1-6 from the timing module.
2. FCNTL1,2 from the front panel.
3. NONE (Always enabled)

The OUTPUT ENABLE signal must be true (high) to enable all eight output drivers. This allows the user to enable or disable the output channels as a synchronous group, simulating the functionality of a data or address bus.

Table 4-1 below illustrates the affects of the PON setting, OUTPUT ENABLE signal and stimulus memory data on the driver output.

PON	OUTPUT ENABLE	STIMULUS MEMORY		DRIVER OUTPUT
		TRI/STATE	OUTPUT	
FALSE (LOW)	X	X	X	High Z
TRUE	FALSE (LOW)	X	X	High Z
TRUE	HIGH/NONE	1	X	High Z
TRUE	HIGH/NONE	0	0	Logic Zero
TRUE	HIGH/NONE	0	1	Logic One

Table 4-1 Driver Output State

4.1.1.4 STIM_LOAD Delay

The STIM_LOAD delay allows the user to adjust the STIM_LOAD signal up to 20ns in 1ns increments.

Delaying the STIM_LOAD signal may be required to allow time for the stimulus memory to be accessed by the rising edge of the STIM_LOAD signal.

Both edges of the STIM_LOAD signal are delayed so that group formatting will not affect the channel pulse width.

4.1.1.5 Mode Enable Source

The mode enable source allows the user to select one of the following sources for the "MODE ENABLE" signal.

1. TSES1-6 from the timing module.
2. FCNTL1,2 from the front panel.
3. NONE

The mode enable signal is only used for the multiplex, serial and increment modes. It functions as a steering signal for the mode logic data registers. See section 4.1.3 for a more detailed description of the "MODE ENABLE" signal.

4.1.2 Stimulus Memory

The stimulus memories on the SR127A consist of two 256K x 16 bit static RAM's. One memory contains the TRISTATE data and the other contains the OUTPUT data. Bits 0 of the tristate memory corresponds to and enables bits 0-3 of the output data. Bits 4 of the tristate memory corresponds to and enables bits 4-7 of the output data. Both of the stimulus memories are addressed by the FMA bus generated from the timing module. Each FMA value causes a new stimulus word.

See section 4.1.1.3 and table 4-1 for the relationship of the output and tristate memory to the driver output.

4.1.3 Stimulus Mode Logic

The mode logic allows the user to select the output mode.

The SR127A has five output modes described below:

1. Standard Stimulus data from memory is direct to the output drivers for parallel output.
2. Multiplex Shifts the data by 8 from bits 15-8 of the stimulus memory into bits 7 to 0 of the output register (i.e. Data shifted out the least significant byte). This doubles the output data rate and the memory depth (512K per channel).
3. Serial Shifts the data by one bit from MSB to LSB of the output register. The LSB channel of the previous I/O module is input into the MSB channel of the next lower I/O module. All 16 bits of the stimulus memory is used for the serial mode.
4. Increment Adds an increment value to the output data to create an incrementing pattern. The carry in and carry out signals can be linked to adjacent modules for larger modulus count.
5. Static Data is loaded from the static register instead of from the stimulus memories.

The multiplex, serial and increment modes are controlled by the "MODE ENABLE" and "STIM_LOAD+D" signals.

The timing relationship between the “MODE ENABLE” and “STIM_LOAD LOAD+D” and their effects on the output data are illustrated in figure 4-4.

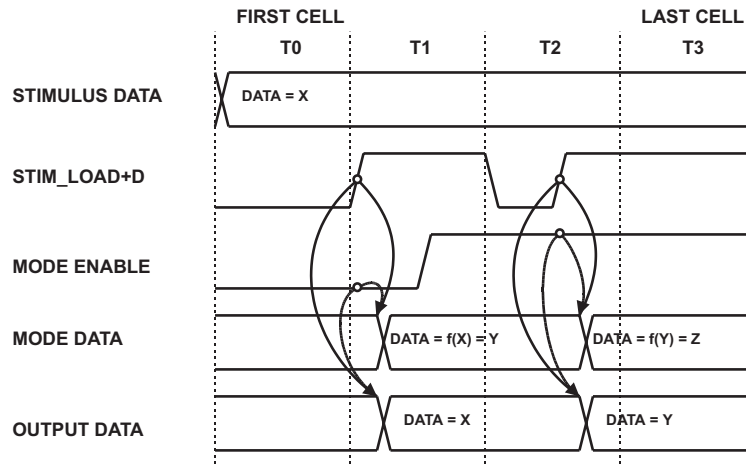


Figure 4-4 Stimulus Signal Timing

The following table describes the timing sequence of the previous figure.

Time	Signal(s)	Condition	Action
T0	-	First Cell Timing Set	• Increments field memory address (FMA) and retrieves stimulus data from OUTPUT and TRISTATE memories.
T1	STIM_LOAD+D	Rising Edge	• In conjunction with "MODE ENABLE" low loads memory data into the output register and then performs the selected mode function, i.e., increment, serial shift or multiplex.
T2	STIM_LOAD+D	Rising Edge	• In conjunction with "MODE ENABLE" high performs mode function on "MODE DATA", i.e., increment, serial shift or multiplex and registers the mode data into the driver output registers.

Table 4-2 Stimulus Signal Timing Description

The following sections will describe each mode including the control signal requirements.

4.1.3.1 Standard Mode

The standard mode routes the stimulus data from the OUTPUT and TRISTATE memories directly to the output drivers.

No timing signals are required for this mode.

Figure 4-3 illustrates the standard mode timing with no group formatting.

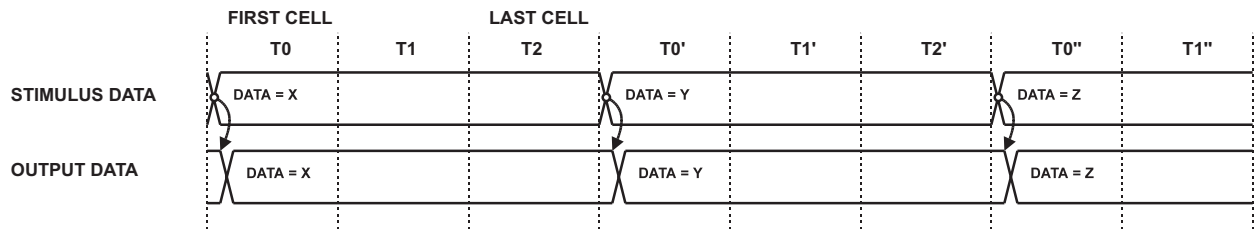


Figure 4-3 Standard Mode Timing

The following table describes the timing sequence of the previous figure.

Time	Signal(s)	Condition	Action
T0	-	First Cell Timing Set	• Increments field memory address (FMA) and retrieves stimulus data from OUTPUT and TRISTATE memories and sends directly to the output drivers.
T0'	-	First Cell Timing Set	• Increments field memory address (FMA) and retrieves stimulus data from OUTPUT and TRISTATE memories and sends directly to the output drivers.
T0''	-	First Cell Timing Set	• Increments field memory address (FMA) and retrieves stimulus data from OUTPUT and TRISTATE memories and sends directly to the output drivers.

Table 4-4 Standard Mode Timing Description

If a bit format is selected, the “STIM_LOAD+D” signal is required, section 4.1.4

4.1.3.2 Multiplex Mode

Multiplex output allows the user to multiplex the 16 X 256K bit data RAM to double the effective memory depth. The lower byte is output first and then swapped with the upper byte.

The “MODE ENABLE” and “STIM_LOAD+D” signals are used to control the multiplex operation and is illustrated in figure 4-5.

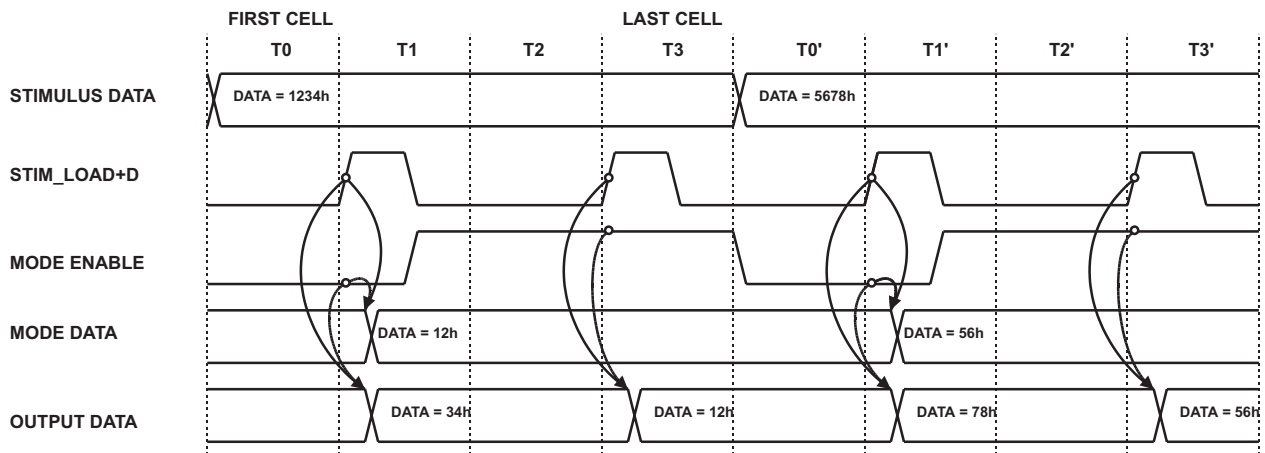


Figure 4-5 Multiplex Mode Timing

The following table describes the timing sequence of the previous figure.

Time	Signal	Condition	Action
T0	-	First Cell Timing Set	• Increments field memory address (FMA) and retrieves stimulus data from OUTPUT and TRISTATE memories (hex 1234).
T1	STIM_LOAD+D	Rising Edge	• In conjunction with “MODE ENABLE” low loads MODE DATA with multiplex shift of STIMULUS DATA (hex 12) and loads OUTPUT DATA with STIMULUS DATA (hex 34).
T3	STIM_LOAD+D	Rising Edge	• In conjunction with “MODE ENABLE” high, loads OUTPUT DATA with MODE DATA (hex 12).
T0'	-	First Cell Timing Set	• Increments field memory address (FMA) and retrieves stimulus data from OUTPUT and TRISTATE memories (hex 5678).
T1'	STIM_LOAD+D	Rising Edge	• In conjunction with “MODE ENABLE” low loads MODE DATA with multiplex shift of STIMULUS DATA (hex 56) and loads OUTPUT DATA with STIMULUS DATA (hex 78).
T3'	STIM_LOAD	Rising Edge	• In conjunction with “MODE ENABLE” high, loads OUTPUT DATA with MODE DATA (hex 56).

Table 4-3 Multiplex Mode Timing Description

4.1.3.3 Serial Mode

Serial mode allows the user to output data from the channel memories through one driver by performing a parallel to serial bit shift of the stimulus memory.

Adjacent I/O modules may be linked to shift data from the other channel memories to the selected lower channel driver for wider parallel data.

The “MODE ENABLE” and “STIM_LOAD+D” signals are used to control the serial operation and is illustrated in figure 4-6.

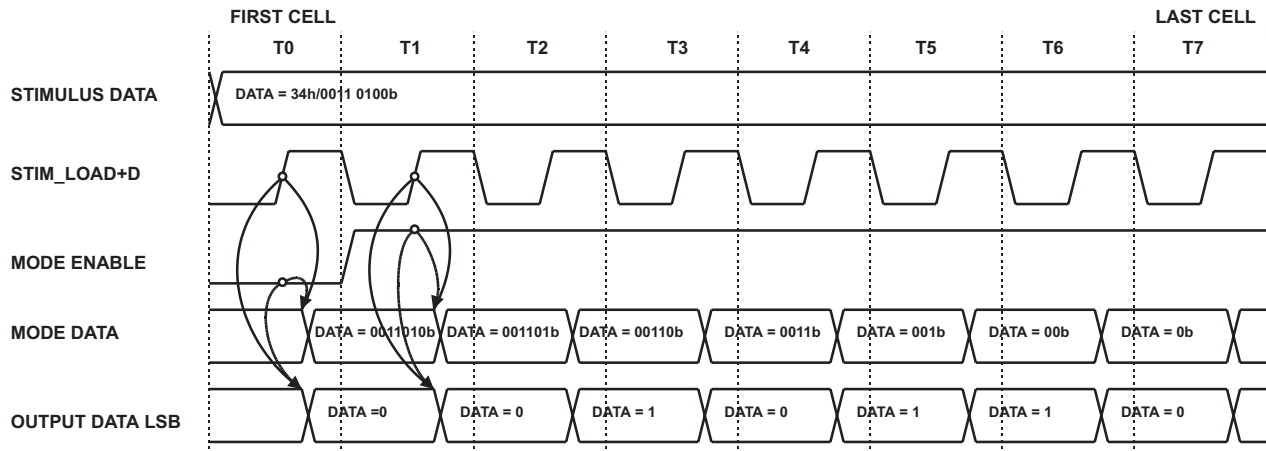


Figure 4-6 Serial Data Output Timing

The following table describes the timing sequence of previous figure.

Time	Signal	Condition	Action
T0	-	First Cell Timing Set	• Increments field memory address (FMA) and retrieves stimulus data from OUTPUT and TRISTATE memories (hex 34, binary 00110100).
T0	STIM_LOAD+D	Rising Edge	• In conjunction with “MODE ENABLE” low loads MODE DATA with serial shift of STIMULUS DATA (hex 1A, binary 0011010) and loads OUTPUT DATA LSB with STIMULUS DATA LSB (0).
T1	STIM_LOAD+D	Rising Edge	• In conjunction with “MODE ENABLE” high loads MODE DATA with serial shift of MODE DATA (hex D, binary 001101) and loads OUTPUT DATA LSB with MODE DATA LSB (0).
T2	STIM_LOAD+D	Rising Edge	• In conjunction with “MODE ENABLE” high loads MODE DATA with serial shift of MODE DATA (hex 6, binary 00110) and loads OUTPUT DATA LSB with MODE DATA LSB (1).
T3	STIM_LOAD+D	Rising Edge	• In conjunction with “MODE ENABLE” high loads MODE DATA with serial shift of MODE DATA (hex 3, binary 0011) and loads OUTPUT DATA LSB with MODE DATA LSB (0).
T4	STIM_LOAD+D	Rising Edge	• In conjunction with “MODE ENABLE” high loads MODE DATA with serial shift of MODE DATA (hex 1, binary 001) and loads OUTPUT DATA LSB with MODE DATA LSB (1).
T5	STIM_LOAD+D	Rising Edge	• In conjunction with “MODE ENABLE” high loads MODE DATA with serial shift of MODE DATA (hex 0, binary 00) and loads OUTPUT DATA LSB with MODE DATA LSB (1).
T6	STIM_LOAD+D	Rising Edge	• In conjunction with “MODE ENABLE” high loads MODE DATA with serial shift of MODE DATA (hex 0, binary 0) and loads OUTPUT DATA LSB with MODE DATA LSB (0).
T7	STIM_LOAD+D	Rising Edge	• In conjunction with “MODE ENABLE” high loads MODE DATA with serial shift of MODE DATA (hex 0, binary 0) and loads OUTPUT DATA LSB with MODE DATA LSB (0), not show in figure.

Table 4-5 Serial Mode Timing Description

4.1.3.4 Increment Mode

The increment mode allows the user to start with an initial value and increment it by 0 to 65,535. This function saves on the use of channel memory.

Adjacent I/O modules can be linked for a wider increment register with carry in/out between modules. The “MODE ENABLE” and “STIM_LOAD+D” signals as well as the increment value are used to control the increment operation and is illustrated in figure 4-7.

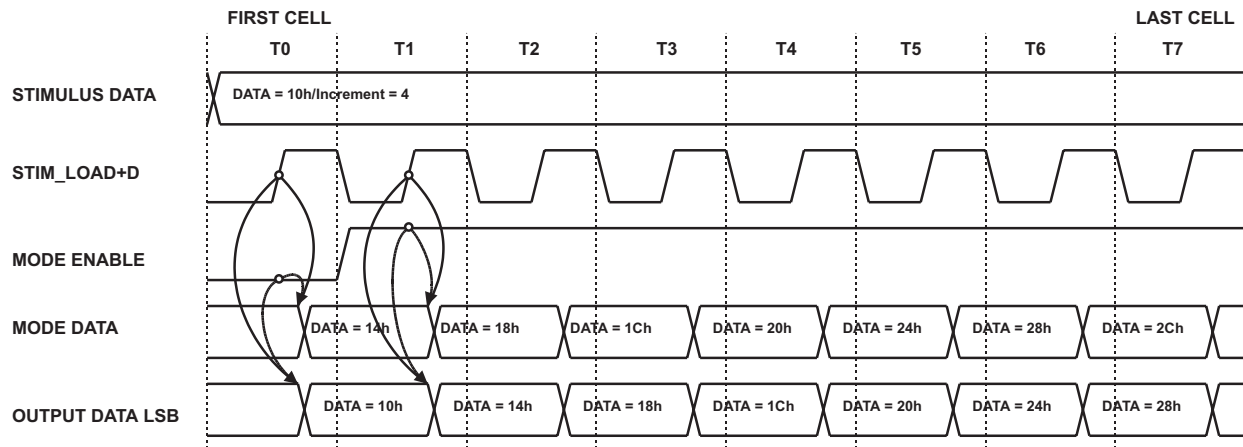


Figure 4-7 Increment Data Output Timing

The following table describes the timing sequence of the previous figure.

Time	Signal	Condition	Action
T0	-	First Cell Timing Set	• Increments field memory address (FMA) and retrieves stimulus data from OUTPUT and TRISTATE memories (hex 10).
T0	STIM_LOAD+D	Rising Edge	• In conjunction with “MODE ENABLE” low loads MODE DATA with increment of STIMULUS DATA (hex 14) and loads OUTPUT DATA with STIMULUS DATA (hex 10).
T1	STIM_LOAD+D	Rising Edge	• In conjunction with “MODE ENABLE” high loads MODE DATA with increment of MODE DATA (hex 18) and loads OUTPUT DATA with MODE DATA (hex 14).
T2	STIM_LOAD+D	Rising Edge	• In conjunction with “MODE ENABLE” high loads MODE DATA with increment of MODE DATA (hex 1C) and loads OUTPUT DATA with MODE DATA LSB (hex 18).
T3	STIM_LOAD+D	Rising Edge	• In conjunction with “MODE ENABLE” high loads MODE DATA with increment of MODE DATA (hex 20) and loads OUTPUT DATA with MODE DATA (hex 1C).
T4	STIM_LOAD+D	Rising Edge	• In conjunction with “MODE ENABLE” high loads MODE DATA with increment of MODE DATA (hex 24) and loads OUTPUT DATA with MODE DATA (hex 20).
T5	STIM_LOAD+D	Rising Edge	• In conjunction with “MODE ENABLE” high loads MODE DATA with increment of MODE DATA (hex 28) and loads OUTPUT DATA with MODE DATA (hex 24).
T6	STIM_LOAD+D	Rising Edge	• In conjunction with “MODE ENABLE” high loads MODE DATA with increment of MODE DATA (hex 2C) and loads OUTPUT DATA with MODE DATA (hex 28).
T7	STIM_LOAD+D	Rising Edge	• In conjunction with “MODE ENABLE” high loads MODE DATA with increment of MODE DATA (hex 30) and loads OUTPUT DATA with MODE DATA (hex 2C).

Table 4-6 Increment Mode Timing Description

4.1.4 Bit Format Logic

This logic performs the bit formatting based on the user selection made in the control logic, section 4.1.1.2.

The falling edge of the “STIM_LOAD” signal controls when the selected formatting is performed. All the output channels share the same group format setting.

A bit format can be applied to any output group regardless of the selected mode.

Figure 4-8 illustrates the group format timing.

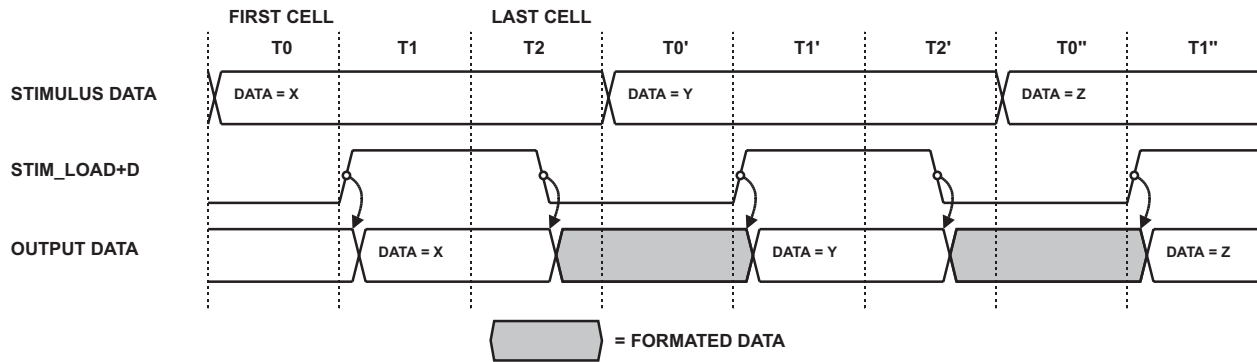


Figure 4-8 Group Format Timing

The following table describes the timing sequence of the previous figure.

Time	Signal	Condition	Action
T0	-	First Cell Timing Set	• Increments field memory address (FMA) and retrieves stimulus data from OUTPUT and TRISTATE memories.
T1	STIM_LOAD+D	Rising Edge	• Loads OUTPUT DATA with STIMULUS DATA.
T2	STIM_LOAD+D	Falling Edge	• Performs the selected format function (RTO, RTZ, RTC, RTT or HOLD).
T0'	-	First Cell Timing Set	• Increments field memory address (FMA) and retrieves stimulus data from OUTPUT and TRISTATE memories.
T1'	STIM_LOAD+D	Rising Edge	• Loads OUTPUT DATA with STIMULUS DATA.
T2'	STIM_LOAD+D	Falling Edge	• Performs the selected format function (RTO, RTZ, RTC, RTT or HOLD).

Table 4-7 Group Format Timing Description

4.2 Response Logic

Figure 4-9 shows the response logic block diagram.

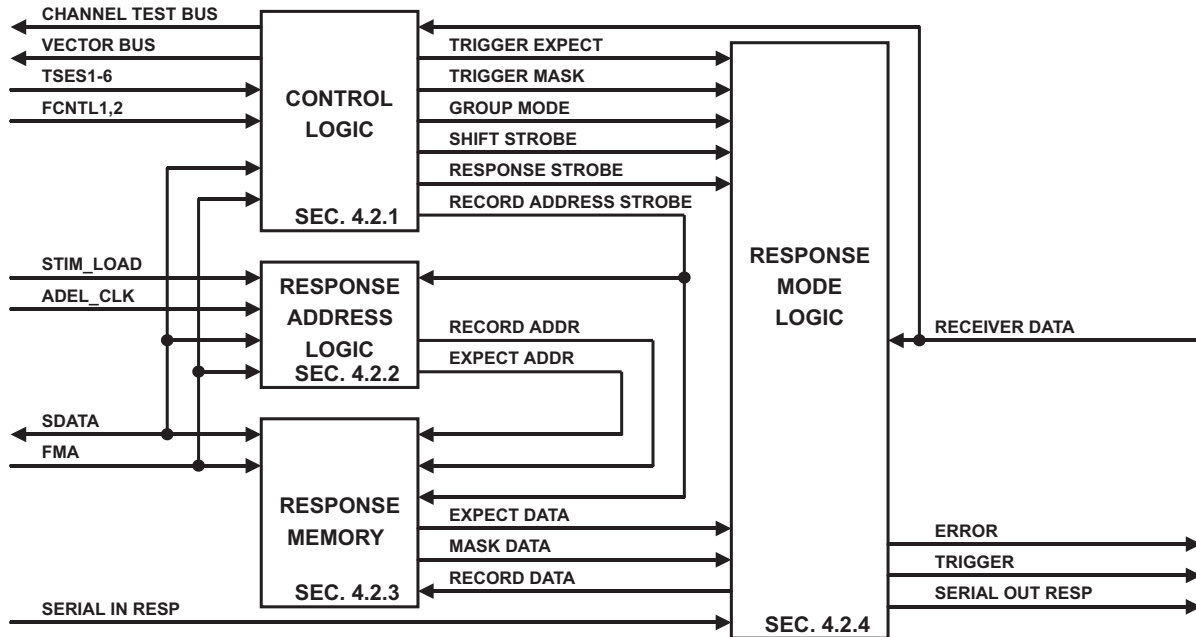


Figure 4-9 Response Logic Block Diagram

The following list describes the functional blocks of figure 4-9 .

- | | | |
|----|------------------------|---|
| 1. | CONTROL LOGIC | Used to select the channel test and vector bus signals, trigger definition, group mode and input strobe selections. The input strobes can also be delayed up to 20ns in 1ns increments. |
| 2. | RESPONSE ADDRESS LOGIC | A series of registers used to delay the FMA in order to generate a synchronous address to the response memories. |
| 3. | RESPONSE MEMORY | Three 256K by 16 memories allows the operator to program real time compare values for the receiver data. |
| 4. | RESPONSE MODE LOGIC | Hardware that processes the response memory based on the selected I/O mode, standard, increment, serial multiplex or static. |

The following list describes the signals shown in figure 4-9 above.

- | | | |
|-----|------------------|--|
| 1. | CHANNEL TEST BUS | The channel test bus allows the user to select two of the receiver channels and route them to the timing module as handshake signals. |
| 2. | VECTOR BUS | The vector bus allows the user to select four of the receiver channels and route them to the timing module as a vector index for the sequence jump logic. |
| 3. | TSES1-6 | Timing set signals that can be selected as either the "SHIFT STROBE", "RESPONSE STROBE" or "RECORD ADDRESS STROBE" by the user. |
| 4. | FCNTL1,2 | Front panel signals that can be selected as either the "SHIFT STROBE", "RESPONSE STROBE" or "RECORD ADDRESS STROBE" by the user. |
| 5. | STIM_LOAD | Timing set signal used to control the response address logic. |
| 6. | ADEL_CLK | Timing set signal used to control the response address logic. |
| 7. | SDATA | Either the baseboard CPU or VXI data bus used to program/query the SR127A. |
| 8. | FMA | Field Memory Address. While running the FMA is generated by the timing module and broadcast to all the I/O modules to select a new response compare word. While not running the FMA is either the baseboard CPU or VXI address bus used to program/query the SR127A. |
| 9. | SERIAL IN RESP | Response data input signal from adjacent higher SR127A for SERIAL function mode. |
| 10. | RECEIVER DATA | Data from the input receivers. |
| 11. | TRIGGER EXPECT | Trigger signal expect data. |
| 12. | TRIGGER MASK | Trigger signal mask data. |
| 13. | GROUP MODE | Selected input mode. |
| 14. | SHIFT STROBE | This signal is used to sample intermediate data for the serial or multiplex mode. |

15.	RESPONSE STROBE	This signal registers the expect, mask and receiver data into the compare register and initiates the real time compare.
16.	RECORD ADDRESS STROBE	The record address strobe disables the record memory and latches the "RECORD ADDR" in the "RESPONSE ADDRESS LOGIC".
17.	RECORD ADDR	Record Memory Address. Delayed FMA bus. Refer to section 4.2.2
18.	EXPECT ADDR	Expect Memory Address. Delayed FMA bus. Refer to section 4.2.2
19.	EXPECT DATA	Response memory expect data addressed by "EXPECT ADDR" and passed to the mode logic.
20.	MASK DATA	Response memory mask data addressed by "EXPECT ADDR" and passed to the mode logic.
21.	RECORD DATA	Data from the input compare register latched by the "RESPONSE STROBE" signal.
22.	ERROR	Registered result of the comparison of the RECEIVER DATA, EXPECT DATA and MASK DATA compared on the rising edge of RESPONSE STROBE.
23.	TRIGGER	Registered result of the comparison of the RECEIVER DATA, TRIGGER EXPECT and TRIGGER MASK compared on the rising edge of RESPONSE STROBE.
24.	SERIAL OUT RESP	Response data output signal to adjacent lower SR127A for SERIAL function mode.

4.2.1 Control Logic

The control logic allows the user to select the vector and channel test bus signals, program the TRIGGER mask and expect registers, select the group input mode and select the input strobes and delays.

4.2.1.1 Vector Bus Select

The vector bus select allows the user to route any of the eight receiver channels to one of the four vector bus signals, VB0 through VB3.

The vector bus is used in conjunction with the SR101A jump logic and indexes a jump table to allow sequence selection based on receiver channel levels.

4.2.1.2 Channel Test Bus Select

The channel test bus select allows the user to route any of the eight receiver channels to one of two channel test bus signals, CHT0 and CHT1.

The channel test bus is used in conjunction with the SR101A timing set test logic to allow timing handshake control based on receiver channel levels.

4.2.1.3 TRIGGER Expect and Mask

The TRIGGER expect and mask are static registers that are programmed for each I/O module. The TRIGGER signal from each module is OR'ed together on the baseboard and routed to the timing module as a test input for the sequence controller or timing generator.

4.2.1.4 Group Mode

The group mode allows the user to select the input mode.

The SR127A has five modes described below:

1. Standard The response strobe latches the data from the receivers and compares the latched data with the mask and expect memories.
2. Multiplex The shift strobe latches the data from the receivers into the lower eight bits of the compare register. The response strobe latches the data from the receivers into the upper eight bits of the compare register and performs the real time compare of the latched data with the mask and expect memories.
3. Serial The shift strobe latches the data from most significant receiver into the MSB of the compare register and then shifts the data by one bit from MSB to LSB. The response strobe latches the data from the most significant receiver into the and performs the real time compare of the latched data with the mask and expect memories. All 16 bits of the response memory are used for the serial mode.
4. Increment The response strobe latches the data from the receivers and compares the latched data with the mask and expect memories.
5. Static Data is latched into the static register instead of the response memories.

4.2.1.5 Input Strobe Source

The input strobe source allows the user to select one of the following sources for the “SHIFT STROBE”, “RESPONSE STROBE” and “RECORD ADDRESS STROBE” signals.

1. TSES1-6 from the timing module.
2. FCNTL1,2 from the front panel.
3. NONE

The rising edge of “RESPONSE STROBE” causes the data from the input receivers to be compared to the data programmed in the EXPECT and MASK memories. The result of the comparison is then stored in the RECORD memory.

The rising edge of “RECORD ADDRESS STROBE” updates the record memory address. The record memory is disabled while the address is updated.

Refer to section 4.2.3 for a description of the response memories.

The multiplex and serial modes use the rising edge of “SHIFT STROBE” to latch and shift the intermediate data.

Table 4-8 below describes the input strobe functions for the group modes.

Group Mode	SHIFT STROBE	RESPONSE STROBE	RECORD ADDRESS STROBE
Standard/Increment	Not Used	Strobe in all eight input register bits, then initiate real-time compare	Strobe “EXPECT ADDR” to the record memory. Record memory writes are disabled while the address is strobed.
Serial	Strobe in most significant channel (MSC) of the channel group into the MSB of the compare register, then shift down by one.	Strobe in MSC of the channel group into the MSB of the input register, then initiate real-time compare.	
Multiplex	Strobe in least significant byte of the channel group into the lower byte of the compare register.	Strobe in least significant byte of the channel group into the upper byte of the compare register, then initiate real-time compare.	

Table 4-8 Shift/Response/Record Address Strobe Functions

4.2.1.6 Input Strobe Delay

The input strobe delay allows the user to adjust the strobe signals up to 20ns in 1ns increments.

4.2.2 Response Address Logic

The response address logic is used to delay the response memory address (EXPECT ADDR) in order to align it with the UUT response data.

Figure 4-10 illustrates the response address logic.

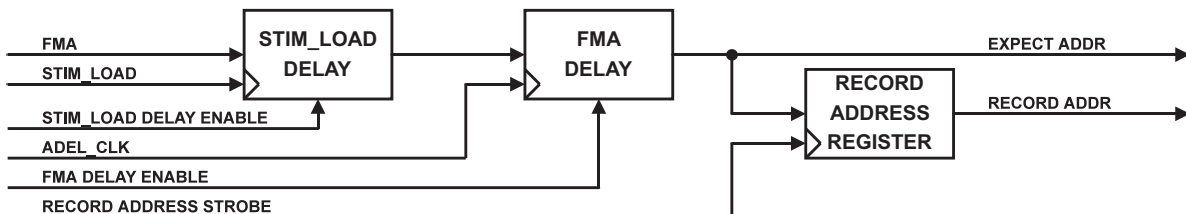


Figure 4-10 Input Address Logic Block Diagram

The following list describes the signals shown in figure 4-10 above.

- | | |
|---|---|
| <ol style="list-style-type: none"> 1. FMA 2. STIM_LOAD 3. STIM_LOAD DELAY ENABLE | <p>Field Memory Address. This group of signals is generated by the timing module and broadcast to the I/O modules. The FMA selects the stimulus/response memory word.</p> <p>Timing module signal that latches the stimulus address bus (FMA) when this delay register is enabled.</p> <p>Control signal used to enable/disable the STIM_LOAD delay register.</p> |
|---|---|

- 4. ADEL_CLK Timing module signal used to latch the FMA delay register.
- 5. FMA DELAY ENABLE Control signal used to enable/disable the FMA delay register.
- 6. RECORD ADDRESS STROBE The record address strobe disables the record memory and latches the "RECORD ADDR".
- 7. EXPECT ADDR This bus addresses the expect and mask response memories.
- 8. RECORD ADDR This bus addresses the record memory.

As shown in figure 4-10 above there are two programmable delay blocks. The combination of these two programmable delays allows the user to select one of four response addressing modes described in the following table 4-9.

Response Delay Mode	Description	Required Timing Signals
None (default)	The response data from the UUT is strobed in the same timing set cycle (Both delay blocks disabled).	None.
Stimulus Offset	The response data from the UUT is strobed prior to the next stimulus pattern output ("STIM_LOAD" delay block enabled).	STIM_LOAD rising edge
FMA Offset	The response data from the UUT is strobed while the next stimulus pattern is output ("FMA" delay block enabled).	None.
Stimulus and FMA Offset	The response data from the UUT is strobed while the next stimulus pattern is output ("FMA" delay block enabled).	STIM_LOAD rising edge

Table 4-9 Response Delay Descriptions

These delay modes are required in stimulus/response applications to keep the response memory synchronized with the stimulus memory.

High speed stimulus/response applications requires unique programming steps to keep the response and stimulus memories synchronized.

4.2.3 Response Memory

The response memories on the SR127A consist of three 256K x 16 bit static RAM's. The first two, EXPECT and MASK contain the data that is used by the input comparator. The third memory, RECORD, is used to store the results of the input comparator. Bit 0 of the EXPECT and MASK is compared with bit 0 of receiver and the result is stored in bit 0 of the RECORD memory.

The mask and expect memories are addressed by the EXPECT ADDR bus. The record memory is addressed by the registered EXPECT ADDR bus called the RECORD ADDR bus.

From the contents of the expect, mask and record memory, two additional "virtual" memories are created, ERROR and RESPONSE.

Table 4-10 below illustrates the real time compare results of the mask and expect memories for each state of the receiver data (logic 0 and logic 1).

COMPARE FUNCTION	MASK MEMORY	EXPECT MEMORY	RECEIVER DATA	RECORD MEMORY	ERROR MEMORY	RESPONSE MEMORY
Expect 0	0	0	Logic 0	0	0	0
			Logic 1	1	1	1
Expect 1	0	1	Logic 0	1	1	0
			Logic 1	0	0	1
Mask off ERROR	1	0	Logic 0	0	0	0
			Logic 1	1	0	1

Table 4-10 Expect, Mask, Record, Error and Response Memory Description

The response memory is the logical “XOR” of the record and expect memories.



Figure 4-13 Response Memory Logic

The error memory is generated by the logical “AND” of the record memory with the complimented mask memory.

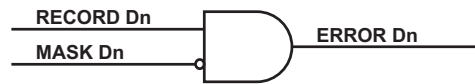


Figure 4-11 Error Memory Logic

4.2.4 Response Mode Logic

The mode of operation for the response logic is the same as the stimulus logic. The data formatting and algorithmic increment modes all record data in parallel. The serial shift function records data only from the most significant channel. The serial multiplex function records data from the least significant byte of the channel group.

Figure 4-12 below is the block diagram for the input mode logic.

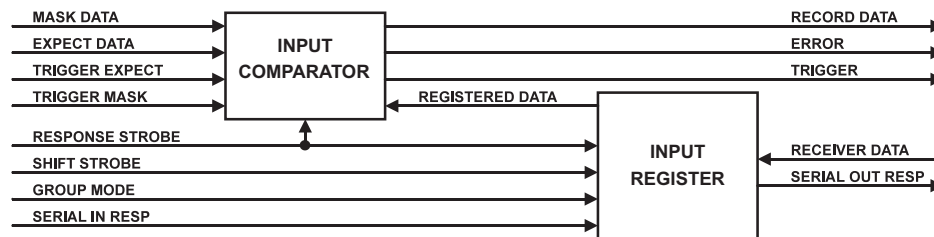


Figure 4-12 Input Mode Logic

The following list describes the functional blocks of figure 4-12.

- | | | |
|----|------------------|--|
| 1. | INPUT COMPARATOR | On the rising edge of the RESPONSE STROBE signal this logic will compare the registered receiver data with the mask and expect memory data and generate the record data and error signal. |
| 2. | INPUT REGISTER | This logic routes the receiver data to the appropriate register based on the selected group and registers the intermediate data on the rising edge of the SHIFT STROBE for the serial and multiplex modes. |

The following list describes the signals shown in figure 4-12 above.

- | | | |
|-----|-----------------|---|
| 1. | MASK DATA | Data from the mask memory. |
| 2. | EXPECT DATA | Data from the expect memory. |
| 3. | TRIGGER EXPECT | Trigger expect register data. |
| 4. | TRIGGER MASK | Trigger mask register data. |
| 5. | RESPONSE STROBE | This signal registers the receiver data and initiates the real time compare. |
| 6. | SHIFT STROBE | This signal is used to record intermediate data from the UUT for the serial and multiplex modes. |
| 7. | GROUP MODE | Selected mode from control logic. |
| 8. | SERIAL IN RESP | Response data input signal from adjacent higher SR127A for SERIAL function mode. |
| 9. | RECORD DATA | Data to the response record memory. |
| 10. | ERROR | Registered signal from the response comparator which indicates that the receiver data did not match the expect and mask data when the response strobe occurred. |
| 11. | TRIGGER | Registered signal from the trigger comparator which indicates that the current response data matches the expect and mask trigger register. |
| 12. | REGISTERED DATA | Input register data. |
| 13. | RECEIVER DATA | Data from the input receivers. |
| 14. | SERIAL OUT RESP | Response data output signal to adjacent lower SR127A for SERIAL function mode. |

4.2.4.1 Input Comparator

The input comparator generates the data for the record memory as well as the ERROR and TRIGGER signals.

Both signals are active high, i.e., a low (0) is false and a high (1) is true.

Bit 0-15 of the mask/expect data is matched with bit 0-15 of the registered data respectively.

Table 4-12 below illustrates the input comparator results for the ERROR and TRIGGER signal.

COMPARE FUNCTION	MASK	EXPECT	REGISTERED DATA	ERROR/TRIGGER
Test for logic 0	0	0	Logic 0	0
			Logic 1	1
Test for logic 1	0	1	Logic 0	1
			Logic 1	0
Mask off ERROR	1	0	Logic 0	0
			Logic 1	0
Not Used	1	1	Logic 0	1
			Logic 1	1

Table 4-12 Input Comparator Results

The expect and mask data from the response memory generates the “ERROR” signal for each memory address. The “TRIGGER” expect and mask data is programmed per module via a static register.

The real time ERROR and TRIGGER signals can be tested by the timing module logic.

The ERROR signal for each channel is registered with the rising edge of the RESPONSE STROBE signal. The ERROR signal for the module is the “OR” of the error signals of the individual channels. Note from table 4-12 that a channel error signal is not generated if the compare is masked off.

The TRIGGER may be the logical “AND” or the logical “OR” of two or more channels.

4.2.4.2 Input Register

The input register logic is used to register data from the input receivers.

The rising edge of RESPONSE STROBE and SHIFT STROBE are used to latch the data.

Table 4-11 shows how RESPONSE STROBE and SHIFT STROBE affect the input registers for the various input modes.

MODE	STROBE	Description
SERIAL	SHIFT	Input register bits 15 through 1 are shifted down by one -and data from either the SERIAL IN DATA or receiver channel 7 is registered in bit 15.
	RESPONSE	Input register bits 15 through 1 are shifted down by one and data from either the SERIAL IN DATA or receiver channel 7 is registered in bit 15. Input register data is then compared against the expect and mask memory.
MULTIPLEX	SHIFT	Receiver channels 7 through 0 are latched into bits 7 through 0 of the input register.
	RESPONSE	Receiver channels 7 through 0 are latched into bits 15 through 8 of the input register. Input register data is then compared against the expect and mask memory.
INCREMENT/ STANDARD	SHIFT	Not used
	RESPONSE	Receiver channels are latched into the input register. Input register data is then compared against the expect and mask memory.

Table 4-11 Input Register Control Signals

4.2.4.3 Response Mode Timing

The response timing is based on the selected address mode (section 4.2.2). The following sections describe the timing restrictions for each mode.

4.2.4.3.1 Default (No Delay) Timing

In this mode the response memories (MASK, EXPECT and RECORD) are synchronous with the stimulus memory.

This is used in applications where the response to a stimulus word can be strobed prior to the end of the stimulus word cycle.

Figure 4-15 illustrates the basic signal relationship of the default input mode:

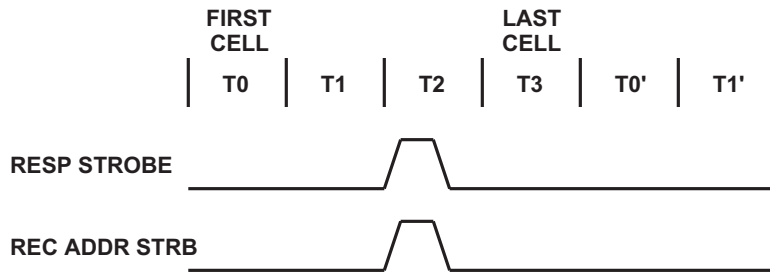


Figure 4-15 Default Timing Restrictions

Refer to the SR192A Timing Manual for timing information and restrictions.

4.2.4.3.2 Stimulus Offset Delay Timing

In this mode the response memories (MASK, EXPECT and RECORD) are delayed by the rising edge of the "STIM_LOAD" signal.

This mode can be used in any stimulus/response applications where the response to a stimulus word can be strobed prior to the output of the next stimulus word.

Figure 4-14 illustrates the basic signal relationship of the stimulus offset input mode:

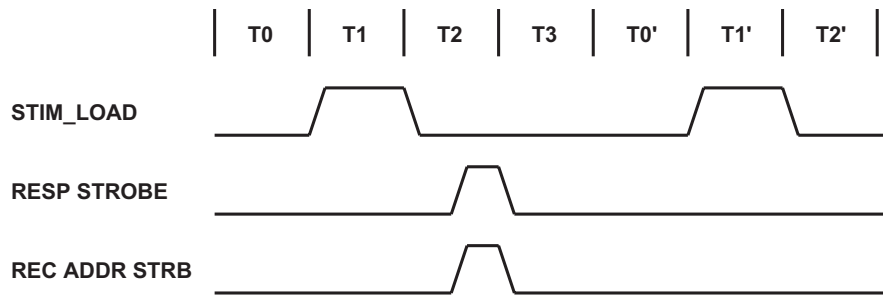


Figure 4-14 Stimulus Offset Delay Timing

Refer to the SR192A Timing Manual for timing information and restrictions.

4.2.4.3.3 FMA Offset Timing

In this mode the response memories (MASK, EXPECT and RECORD) are offset into the next stimulus word.

Figure 4-17 illustrates the basic signal relationship of the default input mode:

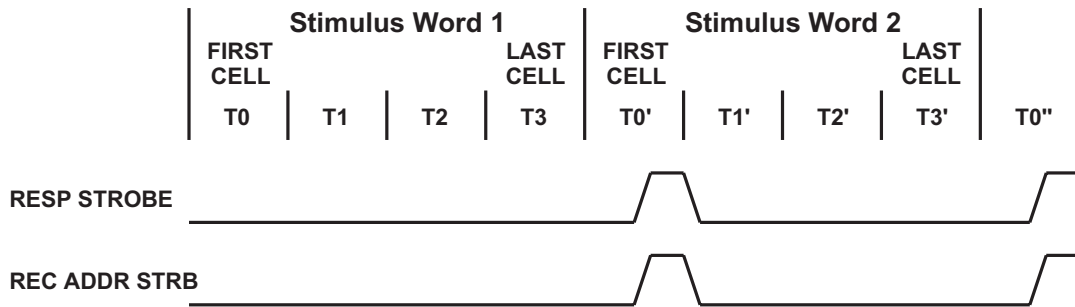


Figure 4-17 FMA Offset Timing Restrictions

Refer to the SR192A Timing Manual for timing information and restrictions.

4.2.4.3.4 Stimulus and FMA Offset Timing

This addressing mode timing is identical to the FMA offset mode. Refer to section 4.2.4.3.3.

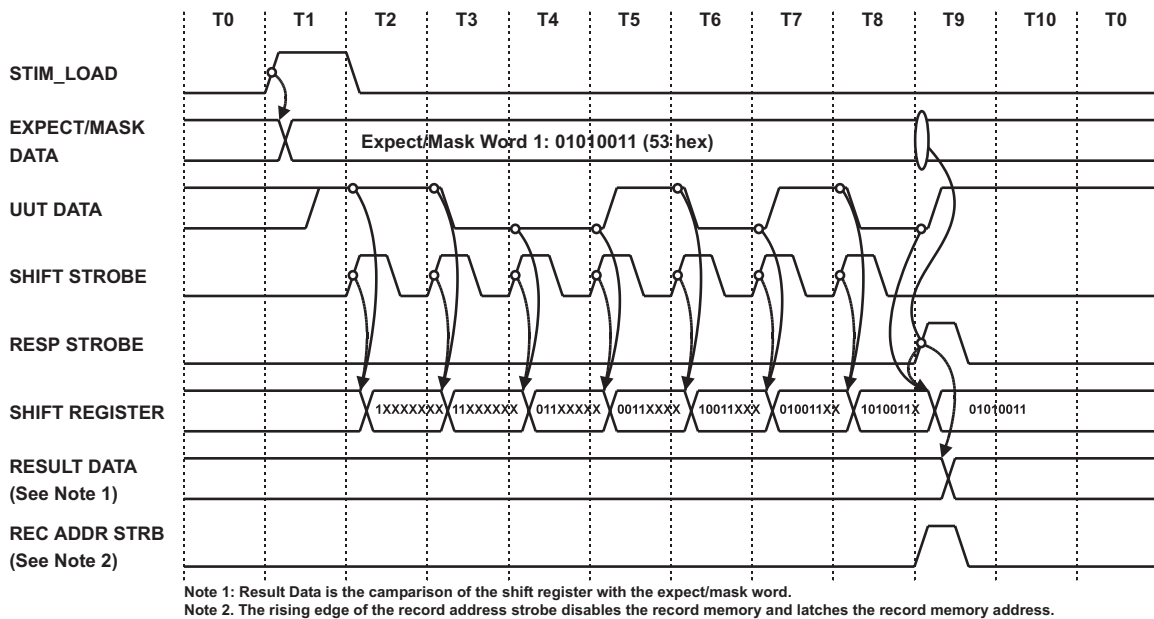
4.2.4.4 Response Mode Timing Examples

The following sections illustrates the timing signal requirements for the SR127A serial and multiplex modes and uses the stimulus offset delay timing.

4.2.4.4.1 Serial Mode Timing

The serial mode allows the operator to input UUT response data as a serial stream. The serial input comes from the most significant channel and is shifted towards the least significant memory bit.

Figure 4-16 illustrates the serial mode response timing.



Note 1: Result Data is the comparison of the shift register with the expect/mask word.
 Note 2: The rising edge of the record address strobe disables the record memory and latches the record memory address.

Figure 4-16 Serial Mode Timing Example

The following table describes the timing sequence in figure 4-16 (Serial Mode Input).

Time	Signal	Condition	Action
T0	-	Start of TS	• Generates new address for stimulus/response memory.
T1	STIM_LOAD	Rising Edge	• Loads Expect/Mask data (Expect/Mask Word 1 in the example) into the response COMPARATOR.
T2	SHIFT STROBE	Rising Edge	• Captures data at MSC and shifts input register by 1 bit toward LSC (data 1XXXXXX in the example).
T3	SHIFT STROBE	Rising Edge	• Captures data at MSC and shifts input register by 1 bit toward LSC (data 11XXXXXX in the example).
T4	SHIFT STROBE	Rising Edge	• Captures data at MSC and shifts input register by 1 bit toward LSC (data 011XXXXX in the example).
T5	SHIFT STROBE	Rising Edge	• Captures data at MSC and shifts input register by 1 bit toward LSC (data 0011XXXX in the example).
T6	SHIFT STROBE	Rising Edge	• Captures data at MSC and shifts input register by 1 bit toward LSC (data 10011XXX in the example).
T7	SHIFT STROBE	Rising Edge	• Captures data at MSC and shifts input register by 1 bit toward LSC (data 010011XX in the example).
T8	SHIFT STROBE	Rising Edge	• Captures data at MSC and shifts input register by 1 bit toward LSC (data 1010011X in the example).
T9	RESP STROBE	Rising Edge	• Captures data at MSC in the shift register. • Captures the mask and expect data in the compare word. • Generates the result data from the shift register and compare word.
	REC ADDR STRB	Rising Edge	• Disables the record memory and latches new address.
T10	-	-	• None.

Table 4-13 Serial Mode Response Timing Description

4.2.4.4.2 Multiplex Mode Timing

The multiplex mode allows the operator to input UUT response data as a multiplex stream. The multiplexed input comes from the lower channel group. The SHIFT_STRB stores the data into the lower eight bits of the input register. The RESP_STRB stores the data into the upper eight bits of the input register.

Figure 4-18 illustrate the multiplex mode response timing.

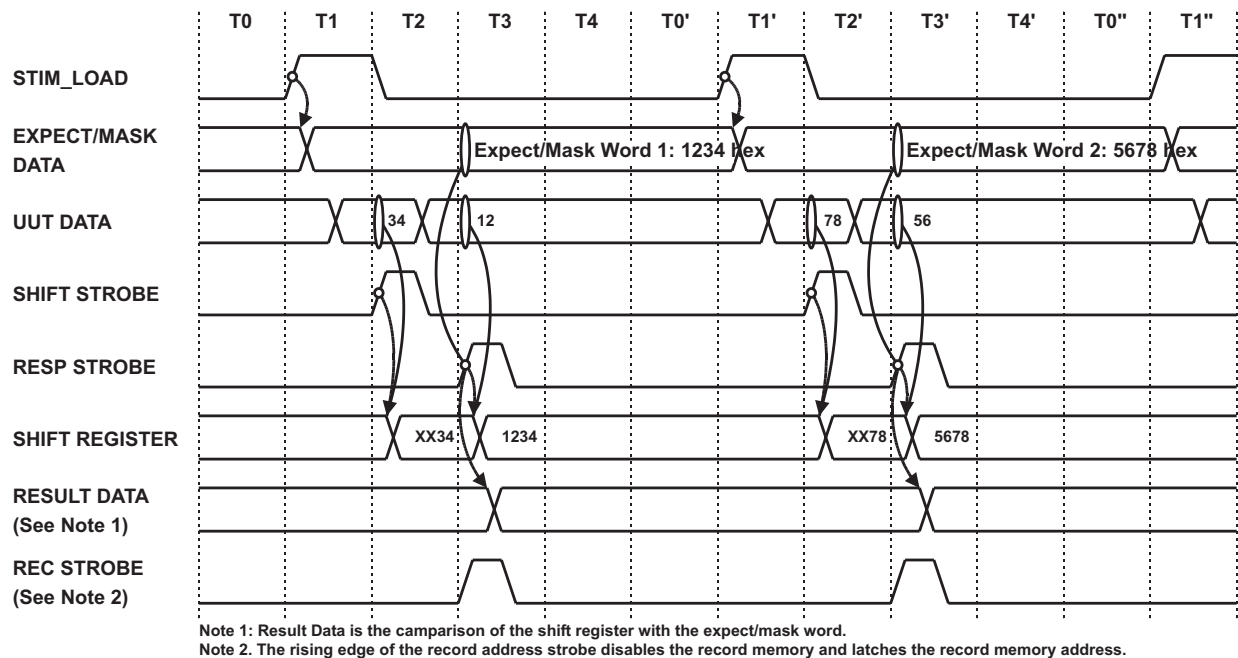


Figure 4-18 Multiplex Mode Response Timing Example

The following table describes the timing sequence in figure 4-18.

Time	Signal	Condition	Action
T0	-	Start of TS	• Generates new address for stimulus/response memory.
T1	STIM_LOAD	Rising Edge	• Loads Expect/Mask data (Expect/Mask Word 1 in the example) into the response comparator.
T2	SHIFT STROBE	Rising Edge	• Captures data and places it in the lower 8 bits of the shift register (data 0xXX34 in the example).
T3	RESP STROBE	Rising Edge	• Captures data and places it in the upper 8 bits of the shift register (data 0x1234 in the example). • Captures the mask and expect data in the compare word. • Generates the result data from the shift register and compare word.
	REC ADDR STRB	Rising Edge	• Disables the record memory and latches new address.
T4	-	-	• None.
T0'	-	Start of TS	• Generates new address for stimulus/response memory.
T1'	STIM_LOAD	Rising Edge	• Loads Expect/Mask data (Expect/Mask Word 2 in the example) into the response comparator.
T2'	SHIFT STROBE	Rising Edge	• Captures data and places it in the lower 8 bits of the shift register (data 0xXX78 in the example).
T3'	RESPONSE STROBE	Rising Edge	• Captures data and places it in the upper 8 bits of the shift register (data 0x5678 in the example). • Captures the mask and expect data in the compare word. • Generates the result data from the shift register and compare word.
	REC ADDR STRB	Rising Edge	• Disables the record memory and latches new address.
T4'	-	-	• None.

Table 4-14 Multiplex Mode Response Timing Description

4.3 Driver/Receiver Logic

The SR127A is an eight channel ECL differential I/O module. Figure 4-19 below illustrates the SR127A's driver/receiver logic.

1 of 2

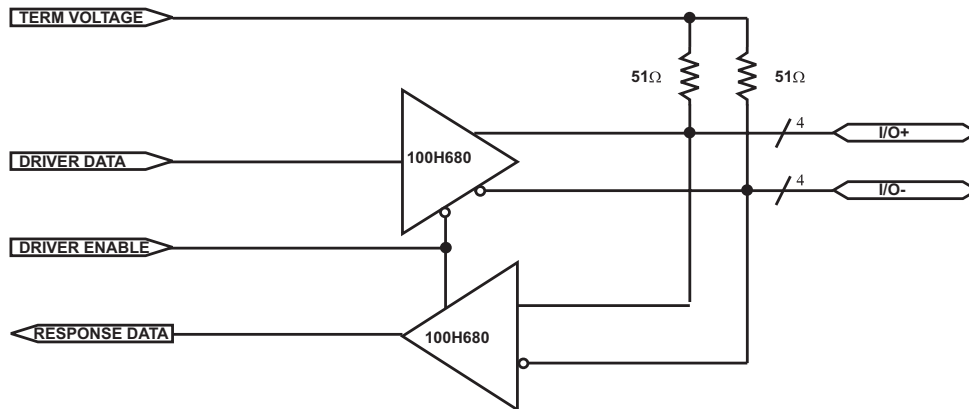


Figure 4-19 SR127A Driver/Receiver Block Diagram

4.3.1 Termination Options

Table 4-15 below describes the termination options for the SR127A.

Channel	Location	Assembly
I/O1+	R7	51.1Ω
I/O1-	R8	51.1Ω
I/O2+	R9	51.1Ω
I/O2-	R10	51.1Ω
I/O3+	R15	51.1Ω
I/O3-	R17	51.1Ω
I/O4+	R21	51.1Ω
I/O4-	R25	51.1Ω
I/O5+	R11	51.1Ω
I/O5-	R12	51.1Ω
I/O6+	R13	51.1Ω
I/O6-	R14	51.1Ω
I/O7+	R16	51.1Ω
I/O7-	R18	51.1Ω
I/O8+	R22	51.1Ω
I/O8-	R26	51.1Ω

Table 4-15 SR127A Termination Options

5 Memory and I/O Front Panel Mapping

Table 5-1 shows the memory and I/O mapping to the front panel.

Memory Bit	DATA	DRA1	DRA2	DRA3	DRA4	DRA5	DRA6	DRB1	DRB2	DRB3	DRB4	DRB5	DRB6
0	I/O1+	CH1	CH17	CH33	CH49	CH65	CH81	CH97	C113	CH129	CH145	CH161	CH177
	I/O1-	CH2	CH18	CH34	CH50	CH66	CH82	CH98	CH114	CH130	CH146	CH162	CH178
1	I/O2+	CH3	CH19	CH35	CH51	CH67	CH83	CH99	CH115	CH131	CH147	CH163	CH179
	I/O2-	CH4	CH20	CH36	CH52	CH68	CH84	CH100	CH116	CH132	CH148	CH164	CH180
2	I/O3+	CH5	CH21	CH37	CH53	CH69	CH85	CH101	CH117	CH133	CH149	CH165	CH181
	I/O3-	CH6	CH22	CH38	CH54	CH70	CH86	CH102	CH118	CH134	CH150	CH166	CH182
3	I/O4+	CH7	CH23	CH39	CH55	CH71	CH87	CH103	CH119	CH135	CH151	CH167	CH183
	I/O4-	CH8	CH24	CH40	CH56	CH72	CH88	CH104	CH120	CH136	CH152	CH168	CH184
4	I/O5+	CH9	CH25	CH41	CH57	CH73	CH89	CH105	CH121	CH137	CH153	CH169	CH185
	I/O5-	CH10	CH26	CH42	CH58	CH74	CH90	CH106	CH122	CH138	CH154	CH170	CH186
5	I/O6+	CH11	CH27	CH43	CH59	CH75	CH91	CH107	CH123	CH139	CH155	CH171	CH187
	I/O6-	CH12	CH28	CH44	CH60	CH76	CH92	CH108	CH124	CH140	CH156	CH172	CH188
6	I/O7+	CH13	CH29	CH45	CH61	CH77	CH93	CH109	CH125	CH141	CH157	CH173	CH189
	I/O7-	CH14	CH30	CH46	CH62	CH78	CH94	CH110	CH126	CH142	CH158	CH174	CH190
7	I/O8+	CH15	CH31	CH47	CH63	CH79	CH95	CH111	CH127	CH143	CH159	CH175	CH191
	I/O8-	CH16	CH32	CH48	CH64	CH80	CH96	CH112	CH128	CH144	CH160	CH176	CH192

Table 5-1 Memory and I/O Front Panel Mapping

Appendix A Glossary of Terms

A16/A24/A32	The VXI address is segmented into three separate areas by a group of VXI signals called the address modifiers (AM0-AM5). These three areas are called A16, A24 and A32. Every VXI module is mapped into 64 bytes of the A16 memory. VXI modules, in addition, may request additional memory map space in the A24 or A32 space. The SR192A maps all the Timing and I/O modules registers into the A24/A32 space.
ADEL_CLK	Address Delay Clock. This signal, generated by the timing generator, clocks the response address delay register on the I/O modules.
CELL	A cell is a single element of a timing set. A timing set can have from 2 to 256 cells. 1 CELL = 1 period of TS_CLK.
CHANNEL TEST	Allows any channel of the installed I/O modules to be used as a test input (TEST1 or TEST2).
ERROR	Registered signal from the response comparator which indicates that the response data did not match the expect and mask data when the input strobe occurred.
FCNTL1/2	Front panel input signals (from the J8 connector) that can be selected to either enable stimulus or strobe response data.
FMA	Field Memory Address. This group of signals is generated by the timing module and broadcast to the I/O modules. The FMA selects the stimulus/response memory word.
FUNCTION CODE(FC)	Each module in a SR192A is assigned a 256K segment of the A32/A24 address map. The 256K can be split into sixteen unique areas via an additional four bits (F0-F3) which is routed to each module. The binary weighted value of the four signals generates sixteen function codes. Each module can define a single register for each function code or an array of 256K registers. Appendix B lists the function codes for this module.
HALF PHASE TIMING	The ability to generate signals that are one-half the period of the TS_CLK. Typically used to enhance the performance of serial operations or to format output data.
HANDSHAKE	Process used to synchronize data to/from a UUT utilizing SR101A timing module test inputs and timing outputs.
I/O CHANNELS	Eight bi-directional data channels per I/O module.
I/O MODULE	Any of Talon's Stimulus/Response modules for the SR192A.
MA_INC	The memory address (FMA) is always incremented at start of each timing cycle (First Cell). The "MA_INC" signal may be used to increment the FMA in later timing cells. The FMA will be incremented at the beginning of the next cell after the "MA_INC". "MA_INC" can be programmed in every other cell except the last two cells.
MODE_EN	Controls the execution of the "Serial", "Multiplex" or "Increment" I/O modes. The MODE_EN source may be one of the TSES1-6 signals, FCNTL1, FCNTL2 or none.

OUTPUT ENABLE	Enable signal. This signal can be used to enable a group of I/O channels. The source of output enable can be a TSES1-6 signal, FCNTL1 or FCNTL2. The enable signal can also be set to "Always" or "Never".
REC ADDR STRB	The record address strobe disables the record memory and latches a new address.
RESPONSE STROBE	This signal registers the Expect, Mask and response data into the compare register and initiates the real time compare.
RESPONSE	The response data of the SR192A is comprised of EXPECT, MASK and RECORD memory.
SADDR	The address bus from the VXI Backplane.
SDATA	The data bus from the VXI Backplane.
SEQUENCE	A sequence is an ordered list of stimulus/response actions consisting of one or more sequence steps.
SEQUENCE STEP	A sequence step is a single element of a sequence. A sequence step selects a timing set, table, loop count, jump condition and control flags.
SHIFT STROBE	This signal is used to sample intermediate data for the serial or multiplex mode.
STIM_LOAD	Timing module control signal that loads the data from the stimulus memory into the output registers. The rising edge of this control signal also registers the stimulus address (FMA) when the output register delay is enabled. The falling edge performs the Data Format function if enabled.
STIMULUS	The stimulus data of the SR192A is determined by the OUTPUT and TRISTATE memory data, output enables, output mode and output format.
TABLE	A table is a defined number of STIMULUS/RESPONSE words. It is located within a specific range of FMA addresses. The FMA range is broadcast to all the I/O modules connected to the timing module.
TIMING MODULE	An SR192A plug-in module that controls stimulus/response timing and sequencing.
TIMING SET	A timing set is the structure that is created that defines the stimulus/response timing. Up to sixteen timing sets can be defined.
TRANSFER	See WORD.
TRISTATE Dn	Tristate driver data from the stimulus memory.
TS_CLK	Timing Set Clock. This signal clocks the timing generator. Each cell is one period of the TS_CLK.
TSES1...6	General purpose Timing Set signals that can be used to enable stimulus drivers, enable mode functions, strobe data into registers or strobe response data into memory.
TSINPUT1/2	Front panel test input signal. Each timing module has two test input signals available, TEST1 and TEST2. Either TSINPUT signal may be routed to TEST1 or TEST2 for Timing Set or Sequence Control.
TSOUT1..5	Timing Set Output One through Five. General purpose output signals generated by the timing module.

VECTOR	A collection of up to four input channels whose High/Low states define a vector with up to sixteen values (one value for each combination of the input levels).
VECTOR BUS	The vector bus is an intermodule bus that connects all of the Series A I/O modules with the associated timing module(s). This bus allows the user to route any channel input to any of the four vector bus lines. The Timing Module allows the user to jump to a sequence address where the four vector bus signals address a LUT to determine the jump address.
WORD	A word is a single element of a table. The width of a word depends on the number and type of I/O modules installed in the SR192A.

Appendix B SR127A Function Code Map

Each SR192A module is assigned a base address in the A24/A32 memory. This base address along with a four bit function code gives each module 4MB of register space.

The following sections describes each of the SR127A function code definitions.

1 Output Data (FC0)

The output data is stored in 256K X 16 bit static memory. Table B-1 shows the bit definitions for the output data.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
O16	O15	O14	O13	O12	O11	O10	O9	O8	O7	O6	O5	O4	O3	O2	O1

Table B-1 Output Data Bit Definitions

Field/Bit Definition:

O1 - O16 Output level bit 1 through 16 (1 = logic high, 0 = logic low), see note 1.

Notes:

- The mapping of the output data to the output channels for this module is determined by the I/O mode as described below:

I/O Mode	Mapping
Standard	O1 through O8 mapped to module channel 1 through 8.
Incr	O1 through O8 mapped to module channel 1 through 8 when MODE_EN is low on rising edge of STIM_LOAD. Module channel 1 through 8 plus increment mapped to module channel 1 through 8 when MODE_EN high on rising edge of STIM_LOAD.
Serial	O1 mapped to module channel 1 and SER_OUT when MODE_EN is low on rising edge of STIM_LOAD. O16 through O1 right shifted when MODE_EN high on rising edge of STIM_LOAD.
Multiplex	O1 through O8 mapped to module channel 1 through 8 when MODE_EN is low on rising edge of STIM_LOAD. O9 through O16 mapped to module channel 1 through 8 when MODE_EN high on rising edge of STIM_LOAD.
Static	Static register output, output data not used.

2 Tristate Data (FC1)

The tristate data is stored in 256K X 16 bit static memory. Table B-2 shows the memory bit definition.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T16	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1

Table B-2 Tristate Data Bit Definitions

Field/Bit Definition:

T1 - T16 Direction bit 1 through 16 (1 = Input (disables output driver), 0 = enable output driver), see note 1.

Notes:

- The mapping of the tristate data to the output channels for this module is determined by the I/O mode as described below:

I/O Mode	Mapping
Standard	T1 mapped to module channels 1 through 4, T5 mapped to module channels 5 through 8.
Incr	T1 mapped to module channels 1 through 4, T5 mapped to module channels 5 through 8.
Serial	T1 mapped to module channel 1 and SEREN_OUT when MODE_EN is low on rising edge of STIM_LOAD. T16 through T1 right shifted when MODE_EN high on rising edge of STIM_LOAD.
Multiplex	T1 mapped to module channels 1 through 4, T5 mapped to module channels 5 through 8 when MODE_EN is low on rising edge of STIM_LOAD. T9 mapped to module channels 1 through 4, T13 mapped to module channels 5 through 8 when MODE_EN high on rising edge of STIM_LOAD.
Static	Static register enable, tristate data not used.

3 Expect Data (FC2)

The expect data is stored in 256K X 16 bit static memory. Table B-3 shows the memory bit definition.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1

Table B-3 Expect Data Bit Definition

Field/Bit Definition:

E1 - E16 Expect bit 1 through 16 (1 = expect logic high when not masked, 0 = expect logic low when not masked), see note 1 of function code 3.

Notes:

- The mapping of the expect data to the input channels for this module is determined by the I/O mode as described below:

I/O Mode	Mapping
Standard	Rising edge of RESP_STRB stores module channel 8 through 1 into the input register bit 7 through 0 and compares E1 through E8 to the input register bits 7 through 0. Rising edge of REC_STRB writes the result of the comparison to the record memory.
Incr	Rising edge of RESP_STRB stores module channel 8 through 1 into the input register bit 7 through 0 and compares E1 through E8 to the input register bits 7 through 0. Rising edge of REC_STRB writes the result of the comparison to the record memory.
Serial	Rising edge of SHIFT_STRB records the serial input (SER_IN or module channel 8) into bit 15 of the input register and right shifts the register. Rising edge of RESP_STRB stores the serial bit into bit 15 of the input register and compares E16 through E1 to the input register bits 15 to 0. Rising edge of REC_STRB writes the result of the comparison to the record memory.
Multiplex	Rising edge of SHIFT_STRB stores module channel 8 through 1 into the input register bits 15 through 8. Rising edge of RESP_STRB stores the module channels 8 through 1 into bits 7 through 0 of the input register and compares E16 through E1 to the input register bits 15 to 0. Rising edge of REC_STRB writes the result of the comparison to the record memory.
Static	Static register, expect data not used.

- Input data in Standard and Increment modes for channels 9 through 16 is always zero.

4 Mask Data (FC3)

The mask data is stored in 256K X 16 bit static memory. Table B-4 shows the memory bit definition.

DELAY LSW Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M16	M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1

Table B-4 Mask Data Bit Definition

Field/Bit Definition:

M1 - M16 Mask bit 1 through 16 (1 = Mask off error, 0 = not masked), see note 1.

Notes:

1. The mask, along with the expect, allows the user to program a realtime compare as described below:

Mask	Expect	Compare
0	0	Expect Logic low
0	1	Expect logic high
1	X	Mask off error

2. The mapping of the mask data to the input channels for this module is determined by the I/O mode as described below:

I/O Mode	Mapping
Standard	Rising edge of RESP_STRB stores module channel 8 through 1 into the input register bit 7 through 0 and compares E1 through E8 to the input register bits 7 through 0. Rising edge of REC_STRB writes the result of the comparison to the record memory.
Incr	
Serial	Rising edge of SHIFT_STRB records the serial input (SER_IN or module channel 8) into bit 15 of the input register and right shifts the register. Rising edge of RESP_STRB stores the serial bit into bit 15 of the input register and compares E16 through E1 to the input register bits 15 to 0. Rising edge of REC_STRB writes the result of the comparison to the record memory.
Multiplex	Rising edge of SHIFT_STRB stores module channel 8 through 1 into the input register bits 15 through 8. Rising edge of RESP_STRB stores the module channels 8 through 1 into bits 7 through 0 of the input register and compares E16 through E1 to the input register bits 15 to 0. Rising edge of REC_STRB writes the result of the comparison to the record memory.
Static	Static register, expect data not used.

3. Input data in Standard and Increment modes for channels 9 through 16 is always zero.

5 Record Data (FC4)

The record data is stored in 256K X 16 bit static memory. The record memory is the result of the expect memory compared with the output of the input receivers. Table 3-5 shows the memory bit definition.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1

Table B-5 Record Data Bit Definition

Field/Bit Definition:

R1 - R16 Record results (1 = error, 0 = compare), see note 1.

Notes:

1. The mapping of the expect data to the input channels for this module is determined by the I/O mode as described below:

I/O Mode	Mapping
Standard	Rising edge of RESP_STRB stores module channel 8 through 1 into the input register bit 7 through 0 and compares E1 through E8 to the input register bits 7 through 0. Rising edge of REC_STRB writes the result of the comparison to the record memory R8 through R1.
Incr	
Serial	Rising edge of SHIFT_STRB records the serial input (SER_IN or module channel 8) into bit 15 of the input register and right shifts the register. Rising edge of RESP_STRB stores the serial bit into bit 15 of the input register and compares E16 through E1 to the input register bits 15 to 0. Rising edge of REC_STRB writes the result of the comparison to the record memory R16 through R1.
Multiplex	Rising edge of SHIFT_STRB stores module channel 8 through 1 into the input register bits 15 through 8. Rising edge of RESP_STRB stores the module channels 8 through 1 into bits 7 through 0 of the input register and compares E16 through E1 to the input register bits 15 to 0. Rising edge of REC_STRB writes the result of the comparison to the record memory R16 through R1.
Static	Static register, expect data not used.

6 Error Memory (FC5)

The error memory is generated from the mask and record memories.

Table B-8 shows the memory bit definition.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ER16	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	ER7	ER6	ER5	ER4	ER3	ER2	ER1

Table B-8 Error Memory Bit Definition

Field/Bit Definition:

ER1 - ER16 Error result (0 = no error, 1 = error).

Notes:

None

7 Response (FC6)

The response memory is generated from the expect and record memories. Table B-6 shows the memory bit definition.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD16	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1

Table B-6 Response Memory Bit Definition

Field/Bit Definition:

RD1-RD16 Response data (0 = logic low, 1 = logic high).

Notes:

None

8 Power Control Register (FC7)

The POWER CONTROL REGISTER manages global module functions associated with operation of the SR127A module hardware, see Table B-7 below.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMS	LNKM	LNKL	LNKN	RREG	NU	ORD	ADR	Reserved (0)	CSFT	CERR	ENR	ENU	ENL		

Table B-7 Power Control Register Bit Definition

Field/Bit Definition:

ENL Output enable bit for lower drivers (0=disabled, 1=enabled).
 ENU Output enable bit for upper drivers (0=disabled, 1=enabled).
 ENR Chip enable bit for all the static RAM (0=disabled, 1=enabled).
 CERR Clear the INPUT, EXPECT and MASK registers. See note 1.
 CSFT Clear the SERIAL SHIFT and MULTIPLEX HOLDING registers. See note 2.
 ADR Address delay register (0 = enabled, 1 = disabled). See note 3.
 ORD Output register delay (0 = enabled, 1 = disabled). See note 4.
 RREG Selects the type of data accessed by reading the FC11 register (raw or registered data) when RUN is true (0 = non-registered, 1 - registered).
 LNKN Link next serial mode (1 = output shift register bit 0 routed to next lower I/O module group, 0 = output shift register bit 0 routed to channel 1 of this I/O module).
 LNKL Link LSB for serial and increment mode (0 = link disabled, 1 = link enabled). See note 5.

LNKM Link MSB for serial and increment mode (0 = link disabled, 1 = link enabled).
See note 5.

SMS Static mode select. See note 6.

Notes:

1. Default = 0. Set to a 1 to asynchronously clear the register, set to 0 for normal operation.
2. Set to a 1 to asynchronously clear the registers, set to 0 for normal operation.
3. The ADR is enabled when the UUT response data is offset from the SR127A stimulus data.
4. The ORD is enabled when the SR127A stimulus data is registered.
5. The MSB and LSB link selects the serial input source and carry input source

I/O Mode	LNKM	LNKL	Description
Serial	Disabled	Disabled	• Lower and upper groups configured as independent.
Serial	Disabled	Enabled	• Lower group linked to upper group.
Serial	Enabled	Disabled	• Lower group configured as independent. • Upper group linked to previous higher group.
Serial	Enabled	Enabled	• Serial Lower group linked to upper group. • Upper group linked to previous higher group.
Increment	Disabled	Disabled	• Carry Input set to 0. Carry Output to next I/O module disabled.
Increment	Disabled	Enabled	• Carry Input set to carry output of previous I/O module. Carry Output to next I/O module disabled.
Increment	Enabled	Disabled	• Carry Input set to 0. Carry Output to next I/O module enabled.
Increment	Enabled	Enabled	• Carry Input set to carry output of previous I/O module. Carry Output to next I/O module enabled.

6. The SMS bits allow the user to override the mode select bits. The following table describes the operation of these bits.

Bit 15	Bit 14	STATIC MODE SELECTION
0	0	Normal operation, MSEL0 and MSEL1 selects the output mode.
0	1	Select output mode two when IDLE or RESET.
1	0	Select output mode two, output mode three selected by MSEL_0 signal.
1	1	Select output mode three.

9 Delay Registers and Look Up Tables (FC8)

The DELAY REGISTERS and LOOK UP TABLES (LUT) allow programming and selection of delays for various clocks and strobes on the SR127A. Each delay has a register to select 1ns increments of that delay. The Lookup Table, or LUT, characterizes that delay so that the selection is reasonably monotonic. Normally the user would select only the delay register as the system firmware initializes the TABLE. Delay registers can be addressed while the unit is running. The mapping to select these registers changes for the RUN state because the Memory Address (MA) bus is used for data output and not available to the SR127A register addressing at that time.

Register Description	Address
Response Strobe Lower Delay	Base + 0x0
Response Strobe Lower Lookup Table	Base + 0x40-0x7E
Response Strobe Upper Delay	Base + 0x80
Response Strobe Upper Lookup Table	Base + 0xC0-0xFE
Shift Strobe Delay	Base + 0x100
Shift Strobe Lookup Table	Base + 0x140-0x17E
Record Address Strobe Delay	Base + 0x180
Record Address Strobe Lookup Table	Base + 0x1C0-0x1FE
Stimulus Load Delay	Base + 0x200
Stimulus Load Lookup Table	Base + 0x240-0x27E
Output Enable Lower Delay	Base + 0x280
Output Enable Lower Lookup Table	Base + 0x2C0-0x2FE
Output Enable Upper Delay	Base + 0x300
Output Enable Upper Lookup Table	Base + 0x340-0x37E

9.1 Delay Registers (FC8:0x0, . . . ,0x300)

The delay registers allow the user to directly program a signal delay or select a pre-defined delay programmed in a lookup table. Table B-9 shows the bit definition of the delay registers.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S	NU		DRS			DATA									

Table B-9 Delay Register Bit Definition

Field/Bit Definition:

DATA	This field is either the lookup table index (S = 1) or the raw data to program into the delay register (S = 0).
DRS	Delay register select, see note 1.
S	This bit selects the delay register data source, (0 = bits 0 to 9 of this register, 1 = bits 0 to 9 of the lookup table indexed by bits 0 to 5 of this register).

Notes:

1. Delay select bits are only active when the timing module is running, allowing access to the delay register.

D13	D12	D11	Register
0	0	0	Response Strobe Lower Delay
0	0	1	Response Strobe Upper Delay
0	1	0	Shift Strobe Delay
0	1	1	Record Address Strobe Delay
1	0	0	Stimulus Load Delay
1	0	1	Output Enable Lower Delay
1	1	0	Output Enable Upper Delay

9.2 Lookup Tables (FC8:0x40-0x7E, . . . ,0x340-0x37E)

The lookup tables are initialized on power up and contain the delay register data to select a delay from 0ns to 20ns in 1ns steps.

Each lookup table contains 32 registers. Each register contains a data value used to generate a specific delay. Register index 0 generates a 0ns delay, Register index 20 generates a 20ns delay.

Table B-10 shows the Delay Register Look Up Tables (LUT) bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU						DATA									

Table B-10 Lookup Table Bit Definition

Field/Bit Definition:

DATA	The raw data to program into the delay register.
------	--

Notes:

None

10 I/O Mode Control (FC9)

The mode control registers control the SR127A modes of operation, including selections for: multiplex and serial I/O, bit formatting, increment control, strobe and enable selections. The following table lists the register offsets for FC9.

Register Description	Address
Channel Mode register 1	Base + 0x0
Channel Mode register 2	Base + 0x2
Signal Select Register 1	Base + 0x4
Signal Select Register 2	Base + 0x6
Increment Register	Base + 0x8
Channel Type	Base + 0xA

The SR127A output is controlled by the mode select signals MSEL_0 and MSEL_1. Four output modes can be defined as illustrated in the following table. Each output mode can select the data source of the output registers.

MSEL_1	MSEL_0	Mode Select
0	0	Output Mode 0, load from RAM into output register
0	1	Output Mode 1, load from selected register into output register using bits from channel mode register 1
1	0	Output Mode 2, load from selected register into output register using bits from channel mode register 2
1	1	Output Mode 3, load from selected register into output register using bits from channel mode register 2

10.1 Channel Mode Register 1 (FC9:0x0)

This register programs the I/O bit format and channel control bits for mode 1. Mode 0 control always loads data from the output and tristate memories. Table B-11 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU	M1U			ORU	FMTU			NU	M1L			ORL	FMTL		

Table B-11 Channel Mode Register 1 Bit Definition

Field/Bit Definition:

FMTL	Bit format for Lower channels, see note 1.
ORL	Output register Lower channels (0 = registered, 1 = non-registered)
M1L	I/O mode Lower channels, see note 2.
FMTU	Bit format for Upper channels, see note 1.
ORU	Output register Upper channels (0 = registered, 1 = non-registered)
M1U	I/O mode Upper channels, see note 2.

Notes:

- The following table lists the bit format selections.

Bit 2	Bit 1	Bit 0	Lower Format	Description
Bit 10	Bit 9	Bit 8	Upper Format	
1	0	0	RTT	Return to Tristate
1	0	1	RTO	Return to One
1	1	0	RTZ	Return to Zero
1	1	1	RTC	Return to Complement
0	X	X	HOLD	Hold current data

- The following table lists the I/O mode selections.

Bit 6	Bit 5	Bit 4	Lower Mode	Description
Bit 14	Bit 13	Bit 12	Upper Mode	
0	0	0	Normal	Data loaded from output and tristate memories
0	0	1	Increment	Data loaded from increment register
0	1	0	Multiplex	Data loaded from multiplex register.
0	1	1	Serial	Data loaded from serial shift register.
1	0	0	Static	Data loaded from static register.
1	0	1	Echo	Data loaded from input register.

10.2 Channel Mode Register 2 (FC9:0x2)

This register programs the channel control bits for mode 2 and 3. Table B-12 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU				M3U				M3L			M2U			M2L	

Table B-12 Channel Mode Register 2 Bit Definition

Field/Bit Definition:

M2L	I/O mode lower channels, see note 1.
M2U	I/O mode upper channels, see note 1.
M3L	I/O mode lower channels, see note 2.
M3U	I/O mode upper channels, see note 2.

Notes:

- The following table lists the I/O mode 2 selection.

Bit 2	Bit 1	Bit 0	Lower Mode	Description
Bit 5	Bit 4	Bit 3	Upper Mode	
0	0	0	Normal	Data loaded from output and tristate memories
0	0	1	Increment	Data loaded from increment register
0	1	0	Multiplex	Data loaded from multiplex register.
0	1	1	Serial	Data loaded from serial shift register.
1	0	0	Static	Data loaded from static register.

- The following table lists the I/O mode 3 selection.

Bit 8	Bit 7	Bit 6	Lower Mode	Description
Bit 11	Bit 10	Bit 9	Upper Mode	
0	0	0	Normal	Data loaded from output and tristate memories
0	0	1	Increment	Data loaded from increment register
0	1	0	Multiplex	Data loaded from multiplex register.
0	1	1	Serial	Data loaded from serial shift register.
1	0	0	Static	Data loaded from static register.

10.3 Signal Select Register 1 (FC9:0x4)

This register programs the response, shift and record address strobe signal source. Table B-13 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RECORD				SHIFT				RESPU				RESPL			

Table B-13 Signal Select Register 1 Bit Definition

Field/Bit Definition:

RESPL	Response strobe lower channels selection, see note 1.
RESPU	Response strobe upper channels selection, see note 1.
SHIFT	Shift strobe selection, see note 1.
RECORD	Record address strobe selection, see note 1.

Notes:

1. The following table lists the signal selections.

LSB+3	LSB+2	LSB+1	LSB	Signal
0	0	0	0	TSES1
0	0	0	1	TSES2
0	0	1	0	TSES3
0	0	1	1	TSES4
0	1	0	0	TSES5
0	1	0	1	TSES6
0	1	1	0	FCNTL1
0	1	1	1	FCNTL2
1	X	X	X	None

10.4 Signal Select Register 2 (FC9:0x6)

This register programs the enable and mode select signal source. Table B-14 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSEL_1				MSEL_0				ENABU				ENABL			

Table B-14 Signal Select 2 Register Bit Definition

Field/Bit Definition:

ENABL Output enable lower channels selection, see note 1.
 ENABU Output enable upper channels selection, see note 1.
 MESL_0 Mode select bit 0, see note 1.
 MESL_1 Mode select bit 1, see note 1.

Notes:

1. The following table lists the signal selections.

LSB+3	LSB+2	LSB+1	LSB	Signal
0	0	0	0	TSES1
0	0	0	1	TSES2
0	0	1	0	TSES3
0	0	1	1	TSES4
0	1	0	0	TSES5
0	1	0	1	TSES6
0	1	1	0	FCNTL1
0	1	1	1	FCNTL2
1	X	X	X	Always enable (low)

10.5 Increment Register (FC9:0x8)

This register is used to define the value that will be added to the output register contents in the "Increment Mode". Table B-15 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INCRU								INCRL							

Table B-15 Increment Register Bit Definition

Field/Bit Definition:

INCRL Increment value lower channels.
 INCRU Increment value upper channels.

Notes:

None

10.6 Channel Type Register (FC9:0xA)

This register is used to select the I/O type (uni-directional, bi-directional). Table B-16 shows the signal select register 1 bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU												RLY4	RLY3	RLY2	RLY1

Table B-16 Channel Type Register Bit Definition

Field/Bit Definition:

- RLY1 Channel 1, 5 type (0 = uni-directional, 1 = bi-directional), see note 1.
- RLY1 Channel 2, 6 type (0 = uni-directional, 1 = bi-directional), see note 1.
- RLY1 Channel 3, 7 type (0 = uni-directional, 1 = bi-directional), see note 1.
- RLY1 Channel 4, 8 type (0 = uni-directional, 1 = bi-directional), see note 1.

Notes:

- The relay connects the specified channels to operate as a bi-directional pair. Care must be taken not to set both channels as output.

11 Vector/Trigger Control (FC10)

The vector/trigger control registers allow the user to program the vector bus channel routing and the static trigger expect and mask values.

Register Description	Address
Channel Test Routing	Base + 0x0
Vector Bit Routing Timing Module A	Base + 0x2
Vector Bit Routing Timing Module B	Base + 0x4
Vector Bit/Channel Test Enables	Base + 0x6
Static Trigger expect	Base + 0x8
Static Trigger masks	Base + 0xA

11.1 Channel Test Routing (FC10:0x0)

This register programs the four inter-module signals assigned to the timing module channel test inputs. Table B-17 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHT2B				CHT1B				CHT2A				CHT1A			

Table B-17 Channel Type Register Bit Definition

Field/Bit Definition:

- CHT1A CHT1A signal selection, see note 1.
- CHT2A CHT2A signal selection, see note 1.
- CHT1B CHT1B signal selection, see note 1.
- CHT2B CHT2B signal selection, see note 1.

Notes:

- The following table shows the I/O channel routing.

LSB+3	LSB+2	LSB+1	LSB	Signal

0	0	0	0	Channel 1
0	0	0	1	Channel 2
0	0	1	0	Channel 3
0	0	1	1	Channel 4
0	1	0	0	Channel 5
0	1	0	1	Channel 6
0	1	1	0	Channel 7
0	1	1	1	Channel 8
1	0	0	0	Channel 9, serial/multiplex mode only
1	0	0	1	Channel 10, serial/multiplex mode only
1	0	1	0	Channel 11, serial/multiplex mode only
1	0	1	1	Channel 12, serial/multiplex mode only
1	1	0	0	Channel 13, serial/multiplex mode only
1	1	0	1	Channel 14, serial/multiplex mode only
1	1	1	0	Channel 15, serial/multiplex mode only
1	1	1	1	Channel 16, serial/multiplex mode only

11.2 Vector Bit Routing Timing Module A (FC10:0x2)

This register programs the four inter-module vector signals assigned to timing module A. Table B-18 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VB3A				VB2A				VB1A				VB0A			

Table B-18 Vector Bit Routing Timing Module A Bit Definition

Field/Bit Definition:

VB0A	Timing Module A VB0 signal selection, see note 1.
VB1A	Timing Module A VB1 signal selection, see note 1.
VB2A	Timing Module A VB2 signal selection, see note 1.
VB3A	Timing Module A VB3 signal selection, see note 1.

Notes:

- The following table shows the I/O channel routing.

LSB+3	LSB+2	LSB+1	LSB	Signal
0	0	0	0	Channel 1
0	0	0	1	Channel 2
0	0	1	0	Channel 3
0	0	1	1	Channel 4
0	1	0	0	Channel 5
0	1	0	1	Channel 6
0	1	1	0	Channel 7
0	1	1	1	Channel 8
1	0	0	0	Channel 9, serial/multiplex mode only
1	0	0	1	Channel 10, serial/multiplex mode only
1	0	1	0	Channel 11, serial/multiplex mode only
1	0	1	1	Channel 12, serial/multiplex mode only
1	1	0	0	Channel 13, serial/multiplex mode only
1	1	0	1	Channel 14, serial/multiplex mode only
1	1	1	0	Channel 15, serial/multiplex mode only
1	1	1	1	Channel 16, serial/multiplex mode only

11.3 Vector Bit Routing Timing Module B (FC10:0x4)

This register programs the four inter-module vector signals assigned to timing module B. Table B-20 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VB3B				VB2B				VB1B				VB0B			

Table B-20 Vector Bit Routing Timing Module B Bit Definition

Field/Bit Definition:

VB0B Timing Module B VB0 signal selection, see note 1.
 VB1B Timing Module B VB1 signal selection, see note 1.
 VB2B Timing Module B VB2 signal selection, see note 1.
 VB3B Timing Module B VB3 signal selection, see note 1.

Notes:

- The following table shows the I/O channel routing.

LSB+3	LSB+2	LSB+1	LSB	Signal
0	0	0	0	Channel 1
0	0	0	1	Channel 2
0	0	1	0	Channel 3
0	0	1	1	Channel 4
0	1	0	0	Channel 5
0	1	0	1	Channel 6
0	1	1	0	Channel 7
0	1	1	1	Channel 8
1	0	0	0	Channel 9, serial/multiplex mode only
1	0	0	1	Channel 10, serial/multiplex mode only
1	0	1	0	Channel 11, serial/multiplex mode only
1	0	1	1	Channel 12, serial/multiplex mode only
1	1	0	0	Channel 13, serial/multiplex mode only
1	1	0	1	Channel 14, serial/multiplex mode only
1	1	1	0	Channel 15, serial/multiplex mode only
1	1	1	1	Channel 16, serial/multiplex mode only

11.4 Vector Bit/Channel Test Enables (FC10:0x6)

This register programs the inter-module signals enable bit. Table B-19 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU				CT2B	CT1B	CT2A	CT1A	VB3B	VB2B	VB1B	VB0B	VB3A	VB2A	VB1A	VB0A

Table B-19 Vector Bit/Channel Test Enables Bit Definition

Field/Bit Definition:

VB0A VB0A enable (0=disables, 1=enabled).
 VB1A VB1A enable (0=disables, 1=enabled).
 VB2A VB2A enable (0=disables, 1=enabled).
 VB3A VB3A enable (0=disables, 1=enabled).
 VB0B VB0B enable (0=disables, 1=enabled).
 VB1B VB1B enable (0=disables, 1=enabled).
 VB2B VB2B enable (0=disables, 1=enabled).
 VB3B VB3B enable (0=disables, 1=enabled).
 CT1A CHT1A enable (0=disables, 1=enabled).
 CT2A CHT2A enable (0=disables, 1=enabled).
 CT1B CHT1B enable (0=disables, 1=enabled).
 CT2B CHT2B enable (0=disables, 1=enabled).

Notes:

None

11.5 TRIGGER Expect Data (FC10:0x8)

This register programs the TRIGGER signal expect value. Table B-22 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

Table B-22 TRIGGER Expect Data Bit Definition

Field/Bit Definition:

E0-E15 TRIGGER signal expect data.

Notes:

1. The TRIGGER signal will go true (high) if the input data matches the expect data.
2. Input data in Standard and Increment modes for channels 9 through 16 are always zero.

11.6 TRIGGER Mask Data (FC10:0xA)

This register programs the TRIGGER signal mask value. Table B-21 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0

Table B-21 TRIGGER Mask Data Bit Definition

Field/Bit Definition:

M0-M15 TRIGGER signal mask data. (0=enable compare against expect, 1=mask off).

Notes:

2. Input data in Standard and Increment modes for channels 9 through 16 are always zero.

12 Static Registers (FC11)

The static register allow the user to program/query the I/O channels when set to static mode.

Register Description		Address
Idle/Reset State	Run State	
Non-registered input	Run Register	Base + 0x0
Registered input	NA	Base + 0x2
Output Data	NA	Base + 0x4
Output Enable	NA	Base + 0x6

12.1 Static Non-Registered Input Data-Non Running (FC11:0x0)

This register queries the non-registered input data when a sequence is not running. Table B-25 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								I7	I6	I5	I4	I3	I2	I1	I0

Table B-25 Static Non-Registered Input Data-Non Running Bit Definition

Field/Bit Definition:

I0-I7 Non registered channel data. (0=logic low, 1=logic high).

Notes:

1. Read only register

12.2 Static Registered Input Data-Non Running (FC11:0x2)

This register queries the registered input data when a sequence is not running. Table B-24 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								RI7	RI6	RI5	RI4	RI3	RI2	RI1	RI0

Table B-24 Static Registered Input Data-Non Running Bit Definition

Field/Bit Definition:

RI0-RI7 Registered channel data. (0=logic low, 1=logic high).

Notes:

1. Read only register

12.3 Static Output Data-Non Running (FC11:0x4)

This register programs the static output data value. Table B-23 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								O7	O6	O5	O4	O3	O2	O1	O0

Table B-23 Static Output Data-Non Running Bit Definition

Field/Bit Definition:

O0-O7 Static output data. (0=logic low, 1=logic high).

Notes:

None

12.4 Static Output Enable Data-Non Running (FC11:0x6)

This register programs the static output enable value. Table B-27 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								E7	E6	E5	E4	E3	E2	E1	E0

Table B-27 Static Output Enable Data-Non Running Bit Definition

Field/Bit Definition:

E0-E7 Static enable data. (0=disables output channel, 1=enable output channel).

Notes:

None

12.5 Static Run Register (FC11:0x0)

This register programs/queries the static run data. Table B-26 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_SEL			NU					DATA							

Table B-26 Static Run Register Bit Definition

Field/Bit Definition:

DATA Data for the specified output register (Write) or data from the input register (Read), see note 1 and 2.

REG_SEL During a write, this field selects the register to be programmed, see note 2.

Notes:

1. While running, a read from this register will return either the non-registered or registered input data. The 'RREG' bit in the "Power Control Register" (FC7) selects which input register is returned, (0 = non-registered, 1 = registered).
2. While running, a write to this register programs the output data/enable register based on the REG_SEL field as follows:

15	14	13	Register
0	0	0	Output Data
0	0	1	NU
0	1	0	Output Enable
0	1	1	NU

13 BIT Registers (FC14)

The SR192A BIT (Built In Test) logic uses a Shift-register sequencer and comparator to verify integrity of various internal bus signals. Writing to each register initializes the specific sequencer to perform the test. The table below lists the BIT registers.

Register Description	Address
Inter-module bus test	Base + 0x0
I/O Control Bus Test	Base + 0x2
I/O Address Bus Test 1	Base + 0x4
I/O Address Bus Test 2	Base + 0x6
Serial Bus Test	Base + 0x8
Extended Test	Base + 0xA

13.1 Inter-module Bus Test (FC14:0x0)

This register returns the inter-module bus test results. Table B-30 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU		SB1	SB0	CTB		CTA		VBB			VBA				

Table B-30 Inter-module Bus Test Bit Definition

Field/Bit Definition:

VBA	Vector bus timing module A bits (0 = pass, 1 = fail).
VBB	Vector bus timing module B bits (0 = pass, 1 = fail).
CTA	Channel test timing module A bits (0 = pass, 1 = fail).
CTB	Channel test timing module B bits (0 = pass, 1 = fail).
SB0	Sequence bit 0
SB1	Sequence bit 1 (1 indicates test has completed).

Notes:

1. The BIT tests require specific timing/table/sequence memory programming.

13.2 I/O Control Bus Test (FC14:0x2)

This register returns the I/O control bus results. Table B-29 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								SB1	SB0	TSES6_1					

Table B-29 I/O Control Bus Test Bit Definition

Field/Bit Definition:

TSES6_1	Timing Set Enable Strobe 6 (bit 5) through 1 (bit 0), (0 = pass, 1 = fail).
SB0	Sequence bit 0
SB1	Sequence bit 1 (1 indicates test has completed).

Notes:

1. The BIT tests require specific timing/table/sequence memory programming.

13.3 I/O Memory Address Bus Test 1 (FC14:0x4)

This register returns the I/O memory address bus 1 results. Table B-28 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MA15_0															

Table B-28 I/O Memory Address Bus Test 1 Bit Definition

Field/Bit Definition:

MA15_0	Memory address bit 15 (bit 15) through 0 (bit 0), (0 = pass, 1 = fail).
--------	---

Notes:

1. The BIT tests require specific timing/table/sequence memory programming.

13.4 I/O Memory Address Bus Test 2 (FC14:0x6)

This register returns the I/O memory address bus 2 results. Table B-33 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU												SB1	SB0	MA17	MA16

Table B-33 I/O Memory Address Bus Test 2 Bit Definition

Field/Bit Definition:

MA16	Memory address bit 16, (0 = pass, 1 = fail).
MA17	Memory address bit 17, (0 = pass, 1 = fail).
SB0	Sequence bit 0
SB1	Sequence bit 1 (1 indicates test has completed).

Notes:

1. The BIT tests require specific timing/table/sequence memory programming.

13.5 Serial Bus Test (FC14:0x8)

This register returns the serial bus results. Table B-32 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									SB1	SB0	CB	SH_IN	IN7	ENIO1	DIO1

Table B-32 Serial Bus Test Bit Definition

Field/Bit Definition:

DIO1	(0 = pass, 1 = fail).
ENIO1	(0 = pass, 1 = fail).
IN7	(0 = pass, 1 = fail).
SH_IN	(0 = pass, 1 = fail).
CB	Carry in from previous I/O module (0 = pass, 1 = fail).
SB0	Sequence bit 0
SB1	Sequence bit 1 (1 indicates test has completed).

Notes:

1. The BIT tests require specific timing/table/sequence memory programming.

13.6 Extended Test (FC14:0xA)

This register queries the extended test results. Table B-31 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU							SB1	SB0	TSO4	NU		FC2	FC1	NU	CLK1

Table B-31 Extended Test Bit Definition

Field/Bit Definition:

CLK1	(0 = pass, 1 = fail).
FC1	FCNTL1 Front Panel (0 = pass, 1 = fail).
FC2	FCNTL2 Front Panel (0 = pass, 1 = fail).
TSO4	TSOUT4 Internal (0 = pass, 1 = fail).
SB0	Sequence bit 0
SB1	Sequence bit 1 (1 indicates test has completed).

Notes:

1. The BIT tests require specific timing/table/sequence memory programming.

14 ID/Revision/Monitor Registers (FC15)

These registers allow the user to query the module type and revision as well as providing internal signal monitoring for factory repair. The table below lists the registers assigned to this function code.

Register Description		Address
Read	Write	
Module ID	Signal Monitor	Base + 0x0
Revision	NA	Base + 0x2

14.1 Module ID (FC15:0x0)

This register contains the ID code for this module so that software can query the instrument configuration. Table B-35 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID								ID							

Table B-35 Module ID Bit Definition

Field/Bit Definition:

ID SR127A Module ID(32h/50d).

Notes:

None

14.2 Revision (FC15:0x2)

This register contains the module revision data so software can query the module version. Table B-34 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VER								REV							

Table B-34 Revision Bit Definition

Field/Bit Definition:

REV Current Module revision.
VER Current Module version.

Notes:

None

14.3 Signal Monitor (FC15:0x0)

This register allows factory technicians to select signals for internal test points. Table B-36 shows the register bit description.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								SIG_SEL							

Table B-36 Signal Monitor Bit Definition

Field/Bit Definition:

SIG_SEL Signal select bits, see note 1.

Notes:

1. The signal select bits programs the monitor test point output.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Signal
0	1	X	0	0	0	0	0	Response Strobe Lower
0	1	X	0	0	0	0	1	Response Strobe Upper
0	1	X	0	0	0	1	0	Shift Strobe
0	1	X	0	0	0	1	1	Record Address Strobe
0	1	X	0	0	1	0	0	Stim Load
0	1	X	0	0	1	0	1	Output Enable Lower
0	1	X	0	0	1	1	0	Output Enable Upper
0	1	X	0	0	1	1	1	MODE_EN1
0	1	X	0	1	0	0	0	MODE_EN2
0	1	X	0	1	0	0	1	STIM_LOAD anded with MODE_EN1
0	1	X	0	1	0	1	0	Carry input
0	1	X	0	1	0	1	1	Carry output
0	1	X	0	1	1	0	0	CH8 response register output.
0	1	X	0	1	1	0	1	CH16 response register output.
0	1	X	0	1	1	1	0	CH15 response register input.
0	1	X	0	1	1	1	1	CH8 response register input.
0	1	X	1	0	0	0	0	Serial input bit LSB
0	1	X	1	0	0	0	1	Serial input MSB
0	1	X	1	0	0	1	0	TRIGGER
0	1	X	1	0	0	1	1	ERROR
0	1	X	1	0	1	0	0	TSOUT4
0	1	X	1	0	1	0	1	TSCLK
0	1	X	1	0	1	1	0	Logic high
0	1	X	1	0	1	1	1	Logic low
0	0	X	X	X	X	X	X	Output is tristated and should be pulled HIGH (3.3V)
1	0	X	X	X	X	X	X	
1	1	X	X	X	X	X	X	

