

REFERENCE MANUAL
Talon Instruments™

SR103

16-Channel TTL
Stimulus/Response Module



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Before undertaking any troubleshooting, maintenance or exploratory procedure, read carefully the **WARNINGS** and **CAUTION** notices.



This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.



If this instrument is to be powered from the AC line (mains) through an autotransformer, ensure the common connector is connected to the neutral (earth pole) of the power supply.



Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adapter. This will defeat the protective feature of the third conductor in the power cord.



Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid "live" circuit points.

Before operating this instrument:

1. Ensure the proper fuse is in place for the power source to operate.
2. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until performance is checked by qualified personnel.

DOCUMENT CHANGE HISTORY

Revision	Date	Description of Change
A	06/12/2009	Document Control release

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1 SR103

1.1. INTRODUCTION

The SR103 is a 16 channel bidirectional TTL stimulus/response module. The logic input/output levels are TTL. Each channel incorporates three 128K memories. These memories are nomenclated the OUTPUT, TRI-STATE and RECORD. Data rates to 25 Mhz are achievable.

1.2. SPECIFICATIONS

Number of bidirectional channels	16
Memories per Output channel.....	2
OUTPUT, TRI-STATE	
Memories per Input channel	1
RECORD	
Memory depth per channel.....	128K
Output Specifications	
Maximum data rate	25.....MHz
Output configuration	Registered or non-registered
Output strobe signal - from timing set	CLK OUTPUT
(common to 8 channels)	
Output enable signal	Select 1 of 4 enable signals
(two from Timing Set, two from Front Panel Connector)	
(common to 8 channels)	
FCNTL1-V	
Input Levels.....	+/- 15 volt
Input Impedance.....	> 50K
The FCNTL1-V signal has the same specifications as the I/O channels of Voltage Group 1 (I/O channels 1-96) (Reference SR104 for detailed specifications).	
FCNTL2-	
Input Levels	TTL
Input Impedance82 ohms
Output slew rate	1 volt/nsec at midpoint
Output impedance	(Four 74AS240's tied in parallel)
Output termination.....	Optional 47 ohm series resistor
Two 16 pin sockets (U8, U10) are provided to install jumper platforms or 47 ohm resistor DIP's. 47 ohm resistors are installed at initial shipment.	
Output current.....	.60 ma

Short circuit protectedyes

Input Specifications

Input impedance.....(one 74AS240 TTL Load)

Two 10 pin SIP sockets (U7, U9) are provided to install pull up, pull down termination resistors. No resistors are provided at initial shipment.

Input strobe signal.....Select 1 of 4 input control signals
(two from Timing Set, two from Front Panel Connector)
(common to 8 channels)

FCNTL1-V

Input Levels.....+/- 15 volt

Input Impedance.....> 50K

The FCNTL1-V signal has the same specifications as the I/O channels of Voltage Group 1 (I/O channels 1-96) (Reference SR104 for detailed specifications).

FCNTL2-

Input LevelsTTL

Input Impedance82 ohms

Power Supply Requirements5 volts

+5 volt power is supplied by the VXI backplane. This may be jumpered to the V+ front panel connector, J10, by cutting the etch between E3, E4, E5, E6 and E11, E12 and installing a jumper between E7, E8 and E9, E10.

V+ supply current220 ma/module
(plus UUT load current)

1.3. SR103 FUNCTIONAL DESCRIPTION

Figure 1-1 depicts the SR103 module in relation to other components of the SR192. Either the SR192 CPU or the VXI interface (A32 space) may read or write data from/to the SR103 memories. When com-

manded to run, the SR100 timing set module generates the high speed addressing and control to the SR103.

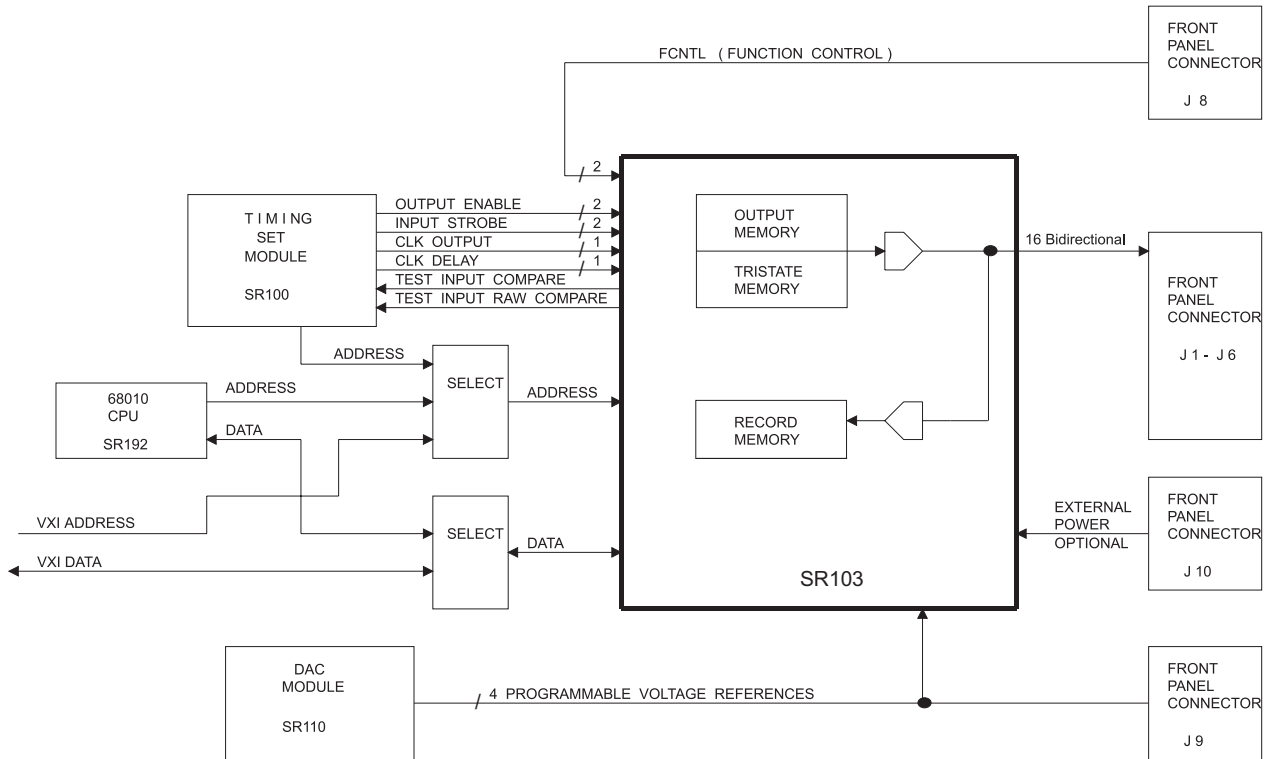


FIGURE 1-1 SR103 BLOCK DIAGRAM

The SR103 consists of two 8 channel groups, each group may select independent enable, and/or strobe signals.

1.3..1 OUTPUT ARCHITECTURE

The output drivers may be configured in one of two modes, either non-registered or registered.

1.3..1.1 OUTPUT NON-REGISTERED OPERATION

Figure 1-2 depicts the non-registered configuration.

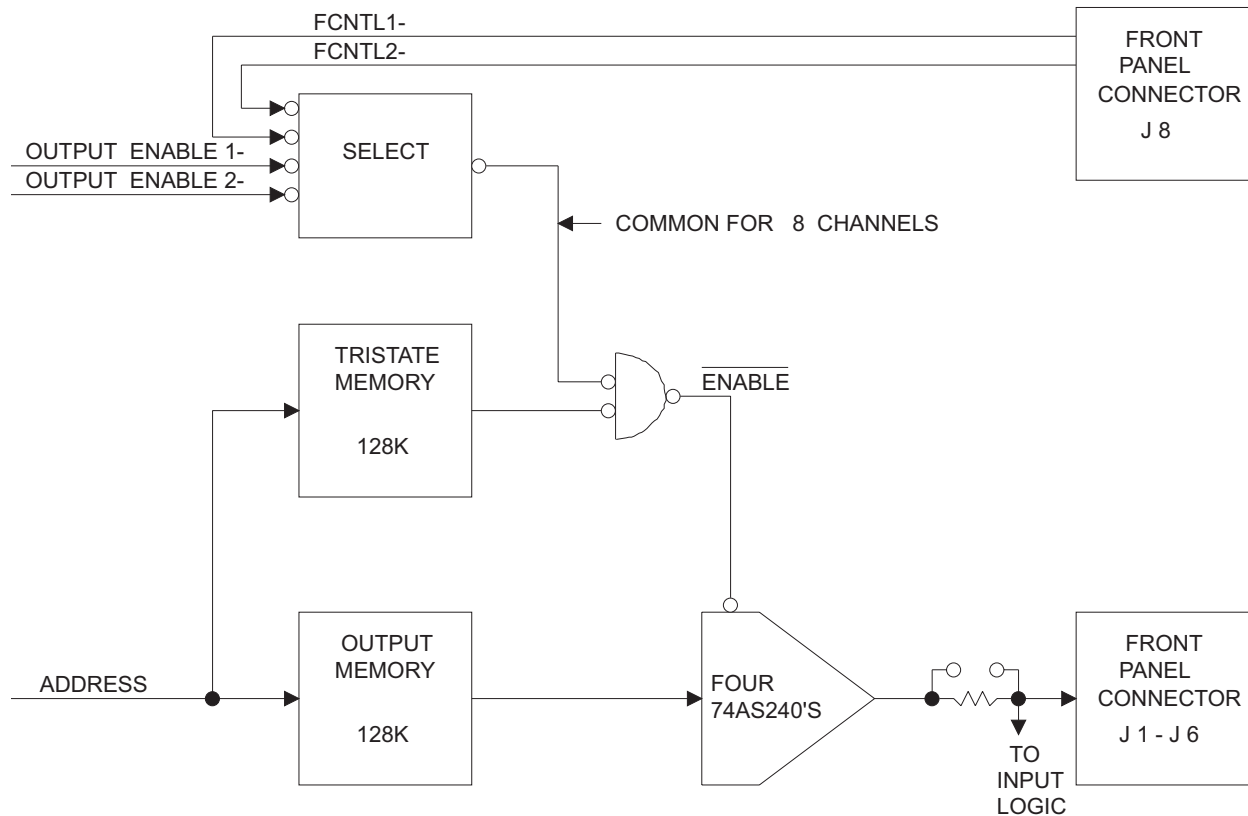


FIGURE 1-2 SR103 OUTPUT LOGIC

When enabled, the output will transition to a high level or low level depending on the state of the OUTPUT MEMORY. A “one” in the OUTPUT MEMORY generates a high level, a “zero” generates a low level. The driver enable signal is generated when the TRI-STATE MEMORY bit is a logic 0 “AND” the selected enable signal (OUTPUT ENABLE 1, 2, or FCNTL 1, 2) is a logic 0.

Typically, for stimulus/response applications the TRI-STATE MEMORY would enable or disable each bit and the selected OUTPUT ENABLE signal would always be a logic 0 (i.e. enabled). For “bus emulation” applications, the TRI-STATE MEMORY would be a logic 0 (i.e. enabled) and the selected OUTPUT ENABLE signal would enable the output at the appropriate time during the “bus” cycle.

For applications where the data is enabled sometime after the beginning of the data period, and disabled sometime before the end of the data period (i.e. bus emulation type applications), the non-registered output data works quite well. For applications where the data is enabled throughout the period, and “glitches” between periods is unacceptable, the output register mode is required.

Data bits 0 through 7 may be enabled independant to data bits 8 through 15.

1.3.1.2 OUTPUT REGISTER OPERATION

Figure 1-3 depicts the output circuit when in the registered mode.

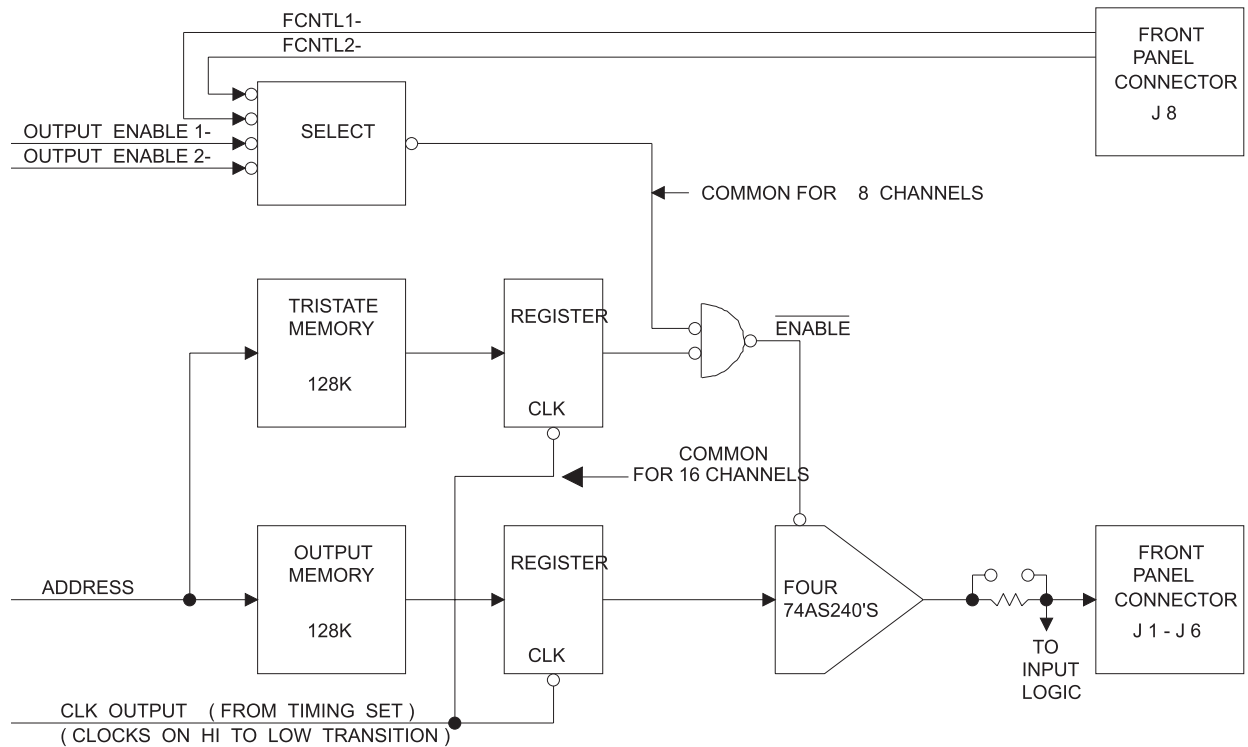


FIGURE 1-3 SR103 REGISTERED OUTPUT LOGIC

The CLK OUTPUT signal generated from the timing set clocks both the output register and the enable register. The registers are clocked on the high to low transition of the respective clock. A minimum delay of one timing cell is required between the timing set CLK SEQUENCE signal and the CLK OUTPUT signal. This time allows for memory access time.

1.3.1.3 TERMINATION

The SR103 incorporates two removable 47 ohm series terminating resistor packs (U8 and U10). Talon ships the SR103 with the terminating resistors installed. They may be removed and must be replaced with a jumper platform.

1.3.2 INPUT ARCHITECTURE

As with the output logic, the input logic may be configured in one of two modes, either registered or non-registered. When the output logic is set to the non-registered mode, the input logic is also set to the non-registered mode (This is done automatically by the SR192 CPU). Conversely, when the output logic is

set to the registered mode, the input logic is also set to the registered mode. Figure 1-4 depicts the input logic when in the non-registered configuration.

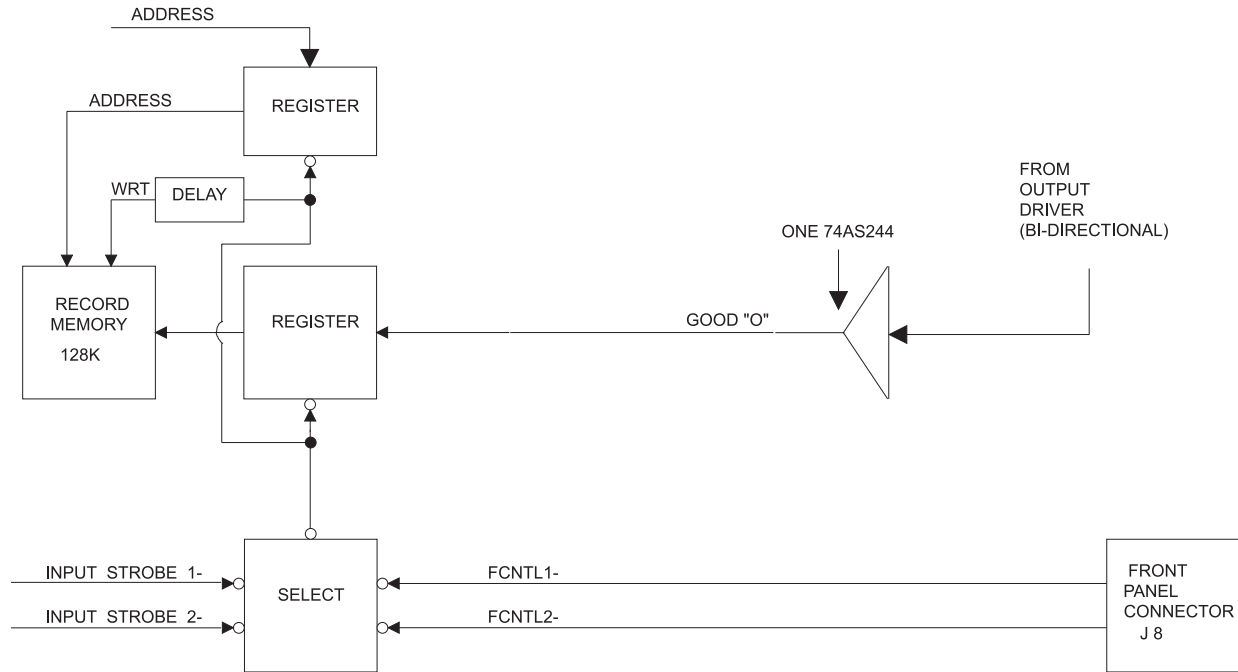


FIGURE 1-4 SR103 INPUT LOGIC

1.3.2.1 INPUT RECEIVERS

The input receivers receive their signals from the SR103 output driver. The function of the input receivers is to convert the users input signals to a good "0" signal. When the input signal is less than .8 volts a "good 0" signal is generated.

The input data, converted to a "good 0" signal is loaded into the RECORD MEMORY after the high to low transition of the sample pulse.

1.3.2.2 INPUT LOGIC REGISTERED MODE

When the output logic is set to the register mode, the input logic is also set to the register mode. The EXPECT and MASK MEMORIES are registered and the RECORD MEMORY Address incorporates an additional register. The functional result from the users standpoint is that he simply needs to know the timing relationship of output data to his input data. Examples of this are given in section 1.3.4 of this write-up.

1.3.2.3 READING THE RECORD MEMORY

The user may read the RECORD MEMORY when in the IDLE timing set cycle or when the timing set is off (program mode).

1.3..2.4 RECORD MEMORY

When reading the RECORD MEMORY, there is no logic function performed on the data (i.e., this is the raw data in the memory). The format for the data is:

0="Good 0"
1="Not "Good 0"

1.3..2.5 DELAY REGISTER

In many high speed applications, the strobe for the input data may need to occur at the very end of the output cycle or even into the following cycle. For these applications, the user must enable the DELAY REGISTER which resides on the SR103. When enabled, the DELAY REGISTER provides a "window" which extends into the following cycle. The user may strobe the input data any time during this window. (Note: The DELAY REGISTER is not shown on the block diagram, figure 4).

Figure 1-5 depicts a window which allows the user to strobe the input data any time from t_{W0} through t_{W1} . The window is created by first enabling the DELAY REGISTER. The CLK DELAY signal from the timing set, reference SR100, defines the t_{W0} to t_{W1} window.

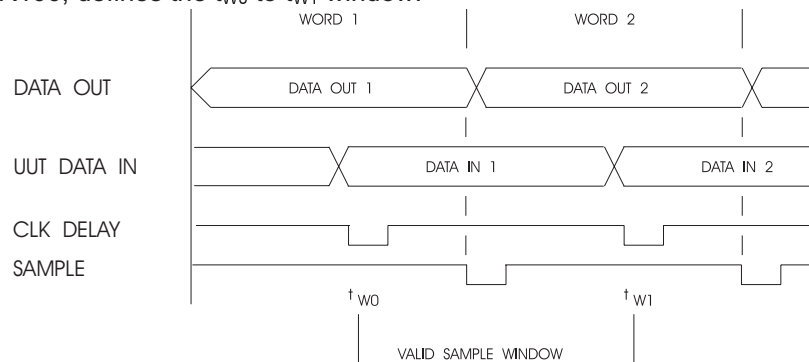


FIGURE 7
FIGURE 1-5

One could take the position that the input data will always occur after the output data, therefore in most applications the DELAY REGISTER could be enabled. This is a valid position and, if implemented, makes the programming of the SR103 more uniform.

NOTE: If the sample pulse occurs in the last cell of a Timing Set, the Delay Register must be enabled and strobed at least one cell prior to the last cell.

1.3..3 APPLICATIONS

The SR103 has been designed to cover a variety of applications. As with many devices, the more versatile the device, the more options the user must specify.

Appendix A depicts twenty-four "modes" which the SR103 could operate in (note that many of these "modes" depend on the clock speed and number of cells in the timing set, not different modes of the SR103). Some of these modes may not make good "application" sense, however they may provide a starting point for any odd user application.

Although Appendix A depicts 24 "modes", there are two basic configurations which cover most applications.

Application 1	STIMULUS/RESPONSE OUTPUT REGISTER ON, DELAY REGISTER ON
Application 2	BUS EMULATION OUTPUT REGISTER OFF, DELAY REGISTER OFF

1.3..3.1 STIMULUS/RESPONSE APPLICATION

This example is for the SR105 which incorporates the EXPECT and MASK memories. The SR103 operates identical except no compare signal is generated.

Figure 1-6 depicts a stimulus/response application. The OUTPUT REGISTER is enabled, which in turn enables the TRI-STATE, EXPECT, and MASK REGISTER. This example assumes the selected OUTPUT ENABLE signal from the timing set is a logic 0 (enabled). The DELAY REGISTER is also enabled, however, since we are strobing the input data in the same cycle as the output, one would accomplish the exact same results with the DELAY REGISTER disabled. This example will be described as time progresses from the Idle Cycle.

- IDLE CYCLE: No data output signal activity. If predetermined data is required in the idle cycle, a CLK OUTPUT signal in Cell 2 of the Idle Cycle is required (i.e. the CLK OUTPUT signal strobes the data residing in the memory at the IDLE WORD).
- WORD1, CELL1: The CLK SEQUENCE signal clocks the SEQUENCE logic which fetches the data for the first word. This word stores the OUTPUT, TRI-STATE, EXPECT and MASK values.
- WORD1, CELL2: The CLK OUTPUT signal strobes the OUTPUT, TRI-STATE, EXPECT and MASK data into their respective registers.
- WORD1, CELL3: The CLK DELAY signal strobes the EXPECT and MASK data into the DELAY REGISTER (sample window register).
- WORD1, CELL5: The selected INPUT STROBE signal samples the input data which in turn generates the compare results. The compare results are loaded into the RECORD MEMORY and the COMPARE signal is transmitted to the TEST INPUT COMPARE signal on the Timing Set.
- WORD1, CELL6: The timing set tests the COMPARE signal for a good compare. If a bad compare is sampled, the timing set hangs up and a timeout condition occurs.
- WORD2, CELL1: The CLK SEQUENCE signal fetches the next word and the process repeats.

This example shows several fundamental rules which must be adhered to when programming the SR103.

- Rule 1: When registered, the CLK OUTPUT signal must occur at least one cell after the CLK SEQUENCE signal (two cells are required at 50 MHz) (Note this rule can be broken if it is acceptable to register the previous word in memory).
- Rule 2: When the DELAY REGISTER is enabled, the CLK DELAY signal must occur at least one cell after the CLK OUTPUT (if Output Register is enabled), or one cell after the CLK SEQUENCE (if Output Register is disabled). (Note, if Output Register is disabled, two cells are required at 50 Mhz).
- Rule 3: If the DELAY REGISTER is enabled, the INPUT STROBE must occur at least one cell after the CLK DELAY. If the DELAY REGISTER is disabled, the input strobe must occur at least one cell after the CLK SEQUENCE (two cells are required at 50 Mhz). Naturally, the Input Data must be stable at the falling edge of the INPUT STROBE.
- Rule 4: Test Input Compare signal must be tested at least one cell after the Input Strobe (two cells are required at 50 MHz).

With these restrictions, it appears it would not be possible to achieve data rates in the 25 MHz range. This is not the case. The sequence logic and timing set logic has been designed such that preamble and postamble sequences can be programmed yielding 25 MHz rates. There are several applications in appendix A which define how this is accomplished.

1.3..3.2 BUS EMULATION APPLICATION

This example is for the SR105 which incorporates the EXPECT and MASK memories. The SR103 operates identical except no compare signal is generated.

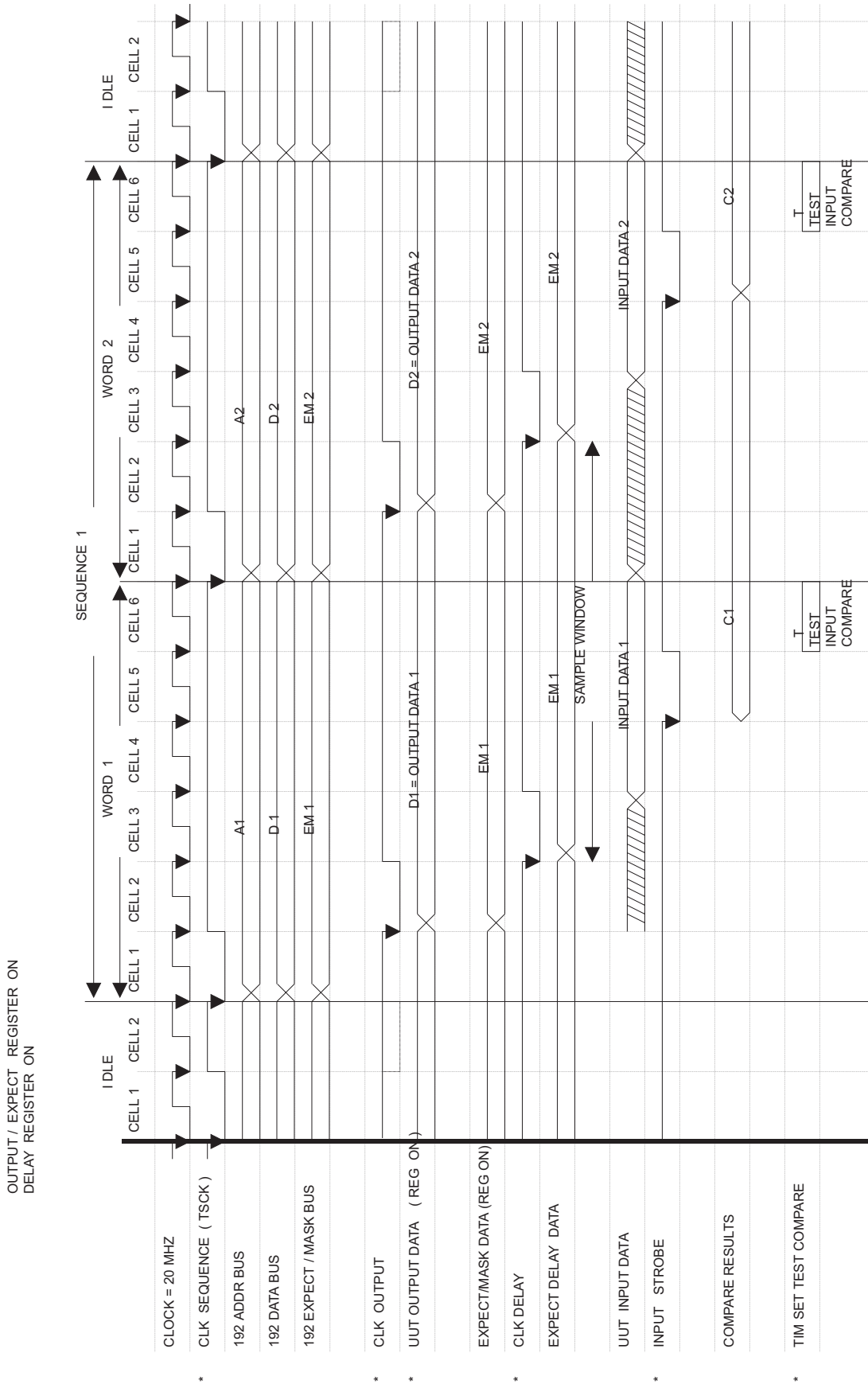


FIGURE 1-6 STIMULUS/RESPONSE APPLICATION

* TIMING SET SIGNAL

Figure 1-7 depicts a Bus Emulation application. In this application, the OUTPUT, TRI-STATE, EXPECT and MASK registers are not enabled. This example also assumes the TRI-STATE MEMORY bit is logic 0 (enabled) for all locations. The DELAY REGISTER is also disabled, however the same results could be achieved with the DELAY REGISTER enabled. This example will be described as time progresses from the Idle Cycle.

IDLE CYCLE: No data output signal activity.

WORD1, CELL1: The CLK SEQUENCE signal clocks the SEQUENCE logic which fetches the data for the first word. This word stores the OUTPUT, TRI-STATE (enabled in this example), EXPECT and MASK values.

WORD1 CELL 3: The selected OUTPUT ENABLE 1 signal in the timing set is activated low. The OUTPUT ENABLE signal enables the output data on the SR103 outputs.

WORD1, CELL5: The selected INPUT STROBE signal samples the input data which in turn generates the compare results. The compare results are loaded into the RECORD MEMORY and the COMPARE signal is transmitted to the TEST INPUT COMPARE signal on the Timing Set.

WORD1, CELL6: The timing set tests the COMPARE signal for a good compare. If a bad compare is sampled, the timing set hangs up and a time-out condition occurs.

WORD2 CELL1: The CLK SEQUENCE signal fetches the next word and the process repeats.

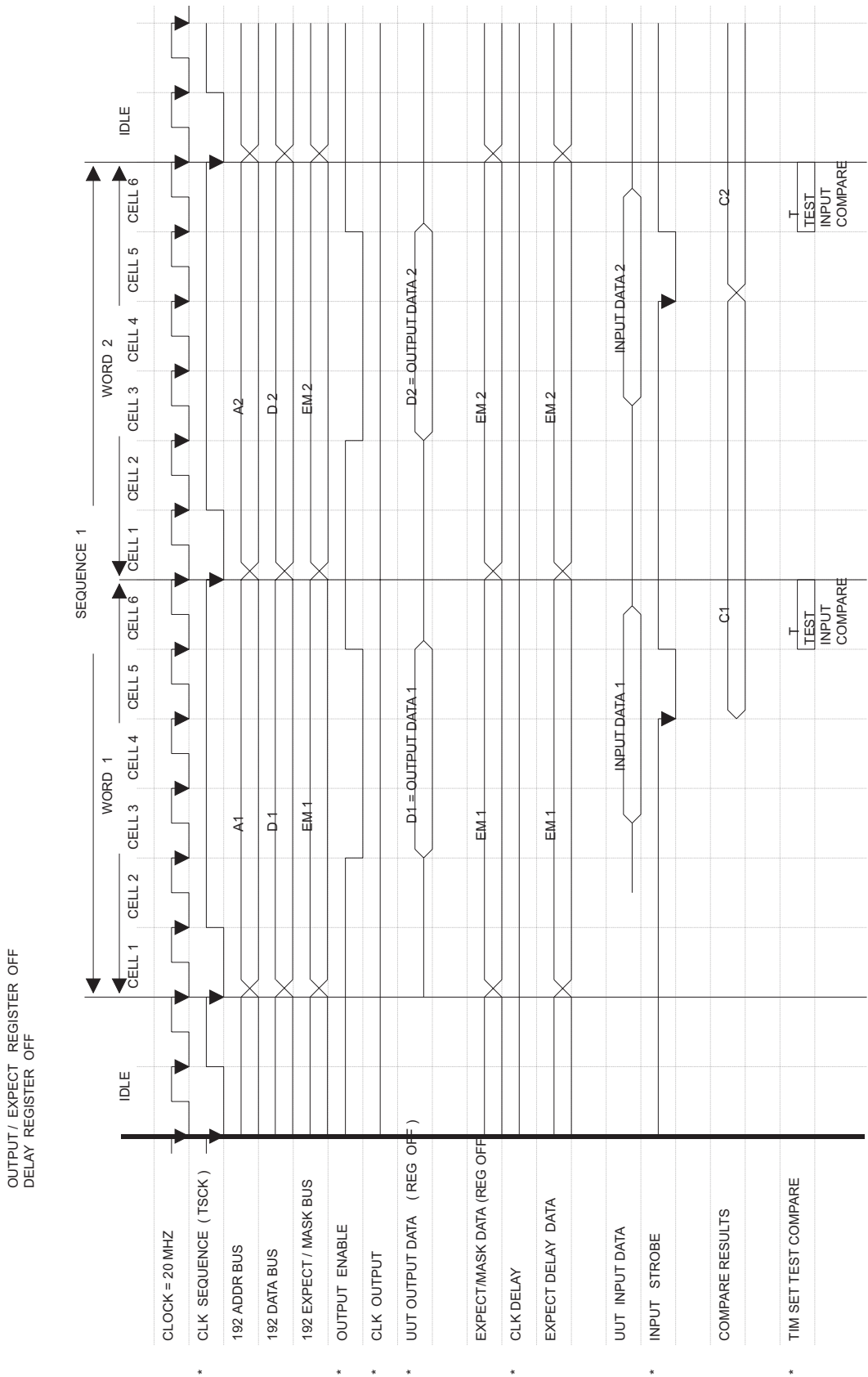


FIGURE 1-7 BUS EMULATION APPLICATION